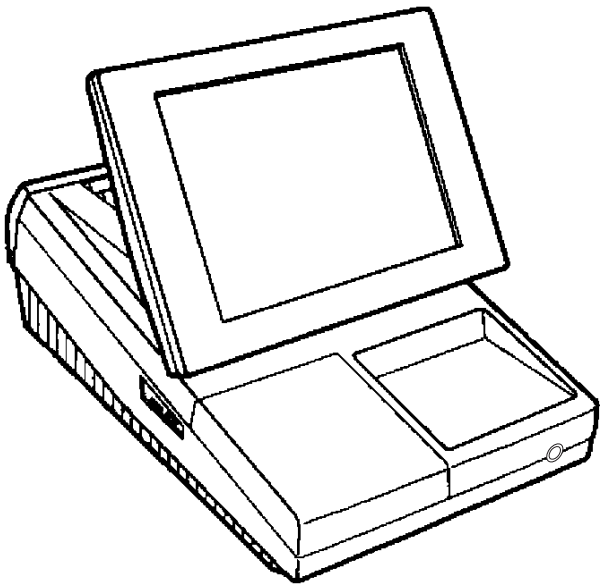
SHARP SERVICE MANUAL

CODE: 00ZUP5300VSME



POS TERMINAL

MODEL UP-5300

("V" version)

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PARTS GUIDE

Parts marked with "⚠" is important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

SHARP CORPORATION

This document has been published to be used for after sales service only.
The contents are subject to change without notice.

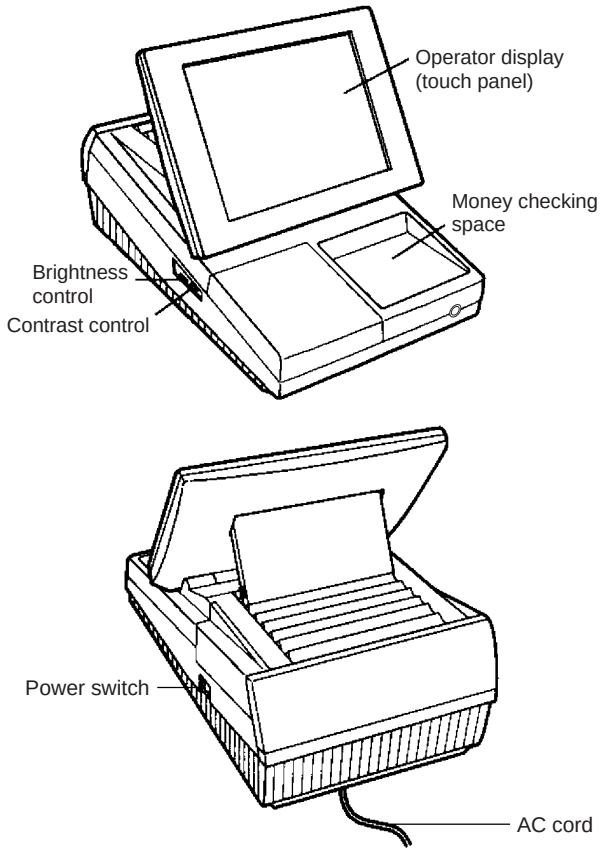
BATTERY DISPOSAL

Contains Nickel Metal Hydride Battery. Must be Disposed of Properly.

Contact Local Environmental Officials for Disposal Instructions.

CHAPTER 1. SPECIFICATIONS

1. Appearance



AC cord

Plug your POS terminal into a wall outlet before using.

Power switch

Set the power switch to the ON (I) position after plugging your POS terminal.

2. Rating

ITEM	SPECIFICATIONS
External dimensions	11.6 (W) × 16.3 (D) × 12.6 (H) in. approximately (295 (W) × 414.5 (D) × 320 (H) mm)
Weight	Approximately 13.9 lb. (5.9 kg)
Power source	220 - 240V AC ± 10%, 60 Hz
Power consumption	Operating : 70W
Working temperature and humidity	32 to 104°F (0 to 40°C) 10 to 90%

3. Hardware

3-1. Display

ITEM	SPECIFICATIONS	NOTE
Type	DSTN color LCD with back light	With 256 colors
Screen size	10.4" Full screen	
Dot format	640 (W) × 480 (H) dots	
Dot size	0.33 × 0.33 mm	
Control	VGA	

3-2. Keyboard

ITEM	SPECIFICATIONS	NOTE
Type	Touch key (Analog touch panel)	
Number of key positions	4096 (W) × 4096 (H) positions	
Control	Mouse emulation	

3-3. PC system

ITEM	SPECIFICATIONS	NOTE
CPU	Pentium processor	
Chip set	FireStar Plus: 82C700U3.2	
Graphic controller	VGAC : MN89305	
Main memory (for executing MS-DOS, Application software)	Standard : 8 Mbytes	EDO type
	Max. : 40 Mbytes	adding S.O.DIMM
Video RAM	1 Mbytes	EDO type
BIOS ROM	512 Kbytes	Flash ROM
OS (MS-DOS) ROM	4 Mbytes	Mask ROM
ROM disk memory (for stored Application software)	Standard : 2 Mbytes	Flash ROM
	Max. : 6 Mbytes	adding UP-F04RB
RAM disk memory (for POS data)	Standard : 1 Mbytes	PS-RAM
	Max. : 3 Mbytes	adding UP-P02MB
Keyboard controller	M38802M270	
Super I/O	M5113 A2	
POS system controller	PSC2 : LZ9AM22	

3-4. Serial port

D-SUB 9-pin connector COM1 and COM2 are equipped.

In order to supply +5V power, CI signal and +5V power supply of COM1 and COM2 can be switched.

2 channels of RJ45 Connector COM port are equipped.

COM3 and COM4 or original I/O address (COM5 and COM6) can be selected as the 2 channels of RJ45 COM port.

COM1 & COM2: D-sub 9 pin			
Pin No.	Signal	Function	I/O
1	CD	Data Carrier Detect	I
2	RD	Receive Data	I
3	SD	Send Data	O
4	ER	Data Terminal Ready	O
5	SG	Signal Ground	—
6	DR	Data set Ready	I
7	RS	Request to Send	O
8	CS	Clear to Send	I
9	CI/+5V	Ring Indicate / +5V	I/–

COM3 or COM5: Modular jack RJ45 8 pin			
Pin No.	Signal	Function	I/O
1	RS	Request to Send	O
2	ER	Data terminal Ready	I
3	SD	Send Data	O
4	SG/(+5V)	Signal Ground/(+5V)	—
5	SG	Signal Ground	–
6	RD	Receive Data	I
7	DR	Data set Ready	I
8	CS	Clear to Send	I

COM4 or COM6: Modular jack RJ45 8 pin			
Pin No.	Signal	Function	I/O
1	RS	Request to Send	O
2	ER	Data terminal Ready	I
3	SD	Send Data	O
4	SG	Signal Ground	—
5	SG	Signal Ground	–
6	RD	Receive Data	I
7	DR	Data set Ready	I
8	CS	Clear to Send	I

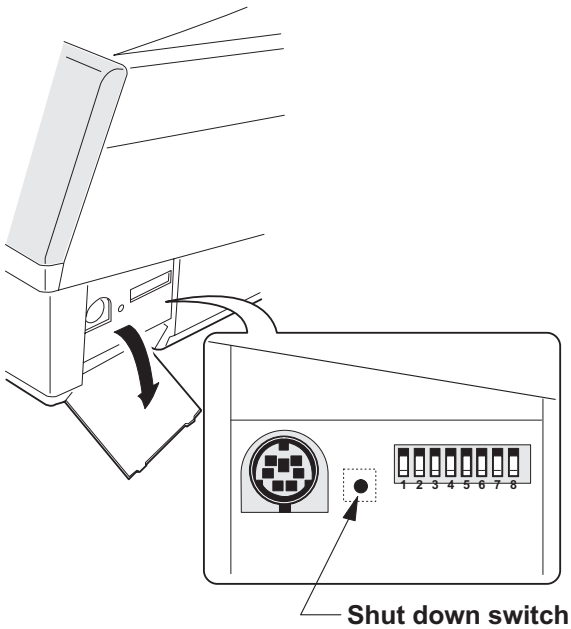
3-5. Expansion slot

ITEM	SPECIFICATIONS	NOTE
Type	ISA bus	Half size PC board
Number of slots	2 slots	
Power consumption	+5V/max. 1.0A	
	+12V/max. 0.05A	

3-6. Shutdown switch

The shutdown switch is used when the OS or application programs are straying and the system can not return to the normal state.

You must not use this shutdown switch when the UP-5300 is running normally. Use this switch only when the main power source is not cut off even if the main unit power switch is set to OFF position. UP-5300 is turned OFF and the hardware is reset by turning the main power switch OFF and then pressing the shutdown switch.



[Out line]

The shutdown switch is single shot type. (Normally OFF position)

Push ON: This position is used to reset stand-by mode for power supply unit when software hang up.

Release OFF: Usually the shutdown switch needs to be set to this position when the UP-5300 is operated.

[Operating method]

The shutdown switch is a push switch. If it is pushed to ON, the UP-5300 stops supplying the power when the power switch is set into stand-by mode.

NOTE: The shutdown operation will be ignored when te power switch is set into power-on position.

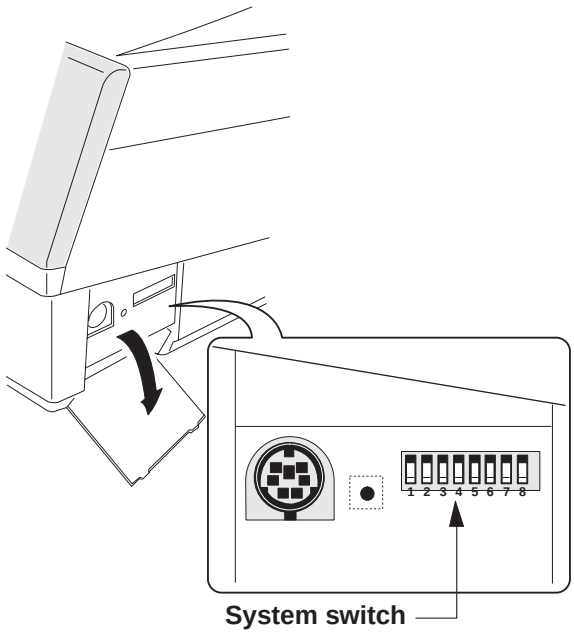
3-7. System switch

The system switches are used to preset various system configurations.

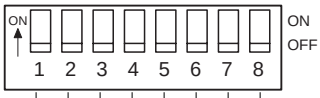
[Out line]

The system switches consists of DIP switches.

[DIP switch]



The PSC2 simply reads the switched signals from the DIP switch as hardware. The meaning of the switch settings are shown on the next page.



: Default setting

DSW-8

Function	OFF (value=1)	ON (value=0)
Serial 3 & 4 decode mode	COM3 & COM4	COM5 & COM6

DSW-7

Function	OFF (value=1)	ON (value=0)
COM3 & COM4 IRQ assign (Serial 3 & 4)	COM3 = IRQ11 COM4 = IRQ10	COM3 = IRQ4 COM4 = IRQ3

DSW-6

Function	OFF (value=1)	ON (value=0)
CMOS Initialize	Not Initialize	Initialize

DSW-5

DSW-4

Drive C:, D: & E: Setting

Drive C:	Drive D:	Drive E:	DSW-4	DSW-5
HDD	—	—	ON (value=0)	ON (value=0)
HDD	PS RAM	Flash ROM	ON (value=0)	OFF (value=1)
PS RAM	Flash ROM	HDD	OFF (value=1)	ON (value=0)
Flash ROM	PS RAM	HDD	OFF (value=1)	OFF (value=1)

DSW-3

Function	OFF (value=1)	ON (value=0)
Boot Drive	Drive A:	Drive C:

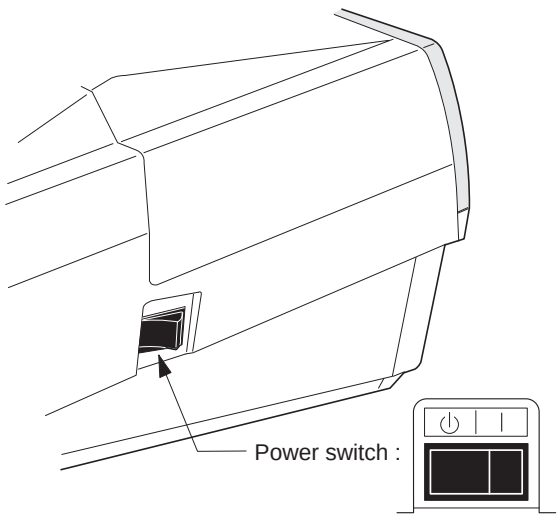
DSW-2

Function	OFF (value=1)	ON (value=0)
Drive A: Device	Mask ROM	FDD

DSW-1

Function	OFF (value=1)	ON (value=0)
Floppy Disk Controller	Not Exit	Exit

3-8. Power switch



[Out line]

The power switch has the positions ON and OFF (Stand-by)

ON position: Usually the power switch needs to be set to this position when the POS-terminal is operated.

OFF position: This position is used to turn the stand-by mode. When the power switch is set to this position, the power supply stops automatically. But if the software program controls the power supply to hold, even if the power switch is set into this position, power is supplied until an software program allows power supply no to hold.

[Operating method]

The power switch is a see-saw switch, and it can be tipped toward the ON or OFF.

4. Software

4-1. Software Structure

The basic system software mainly consists of the following 3 modules.

(1) MS-DOS Version 6.22

The operating system (MS-DOS Version 6.22) is stored in a MROM disk.

(2) Drivers

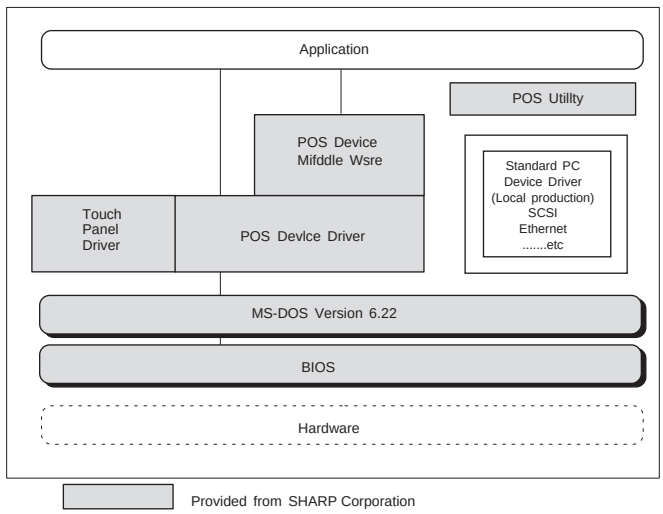
There are following types of drivers

- POS Device Drivers (for Clerk, Buzzer, Drawer, Timer, MCR, Line Display, Serial Port) POS device drivers adopt the same control method as previous (ER-A850/A880/UP-5700) softwares.
- Touch Panel Driver

(3) POS Device Middleware

The middleware has been developed to improve the performance of applications.

(4) Software Structure



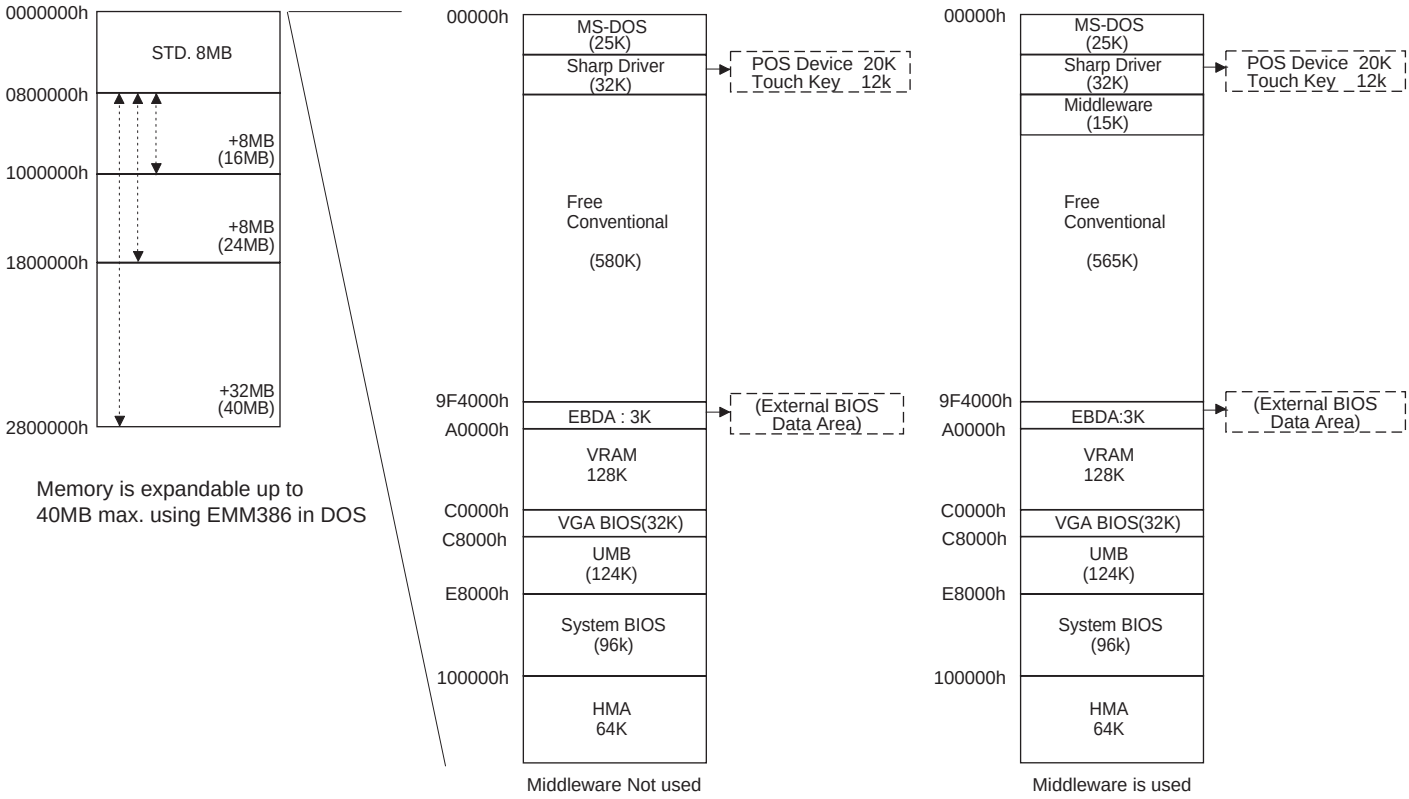
4-2. Basic system software list

ITEM	CONTENTS	for UP-5300	for PC
BIOS (FROM)	• AT compatible system BIOS • VGA BIOS for MN89305 VGA LSI • Standard SETUP program • Flash Disk/MROM Disk/PSRAM Disk built-in control program • Memory size/HDD type auto detect function • No APM/PnP support	○	—
OS (MROM disk)	MS-DOS Version 6.22 (Subset)		
Install program (MROM disk)	• System Install program		
	• APL Install program (for MS-DOS/Windows 95/98/NT)	—	○
POS device driver	• POS device driver	○	—
	• Touch panel driver (mouse emulation I/F only)	○	—
Middleware software and application development tools	• POS device MiddleWare	○	—
	• Printer Logo image loading utility program (MS-DOS/Windows 95)	○	○
	• Touch panel calibration utility program (MS-DOS)	○	—

... These software are provided with FD from SHARP corporation.

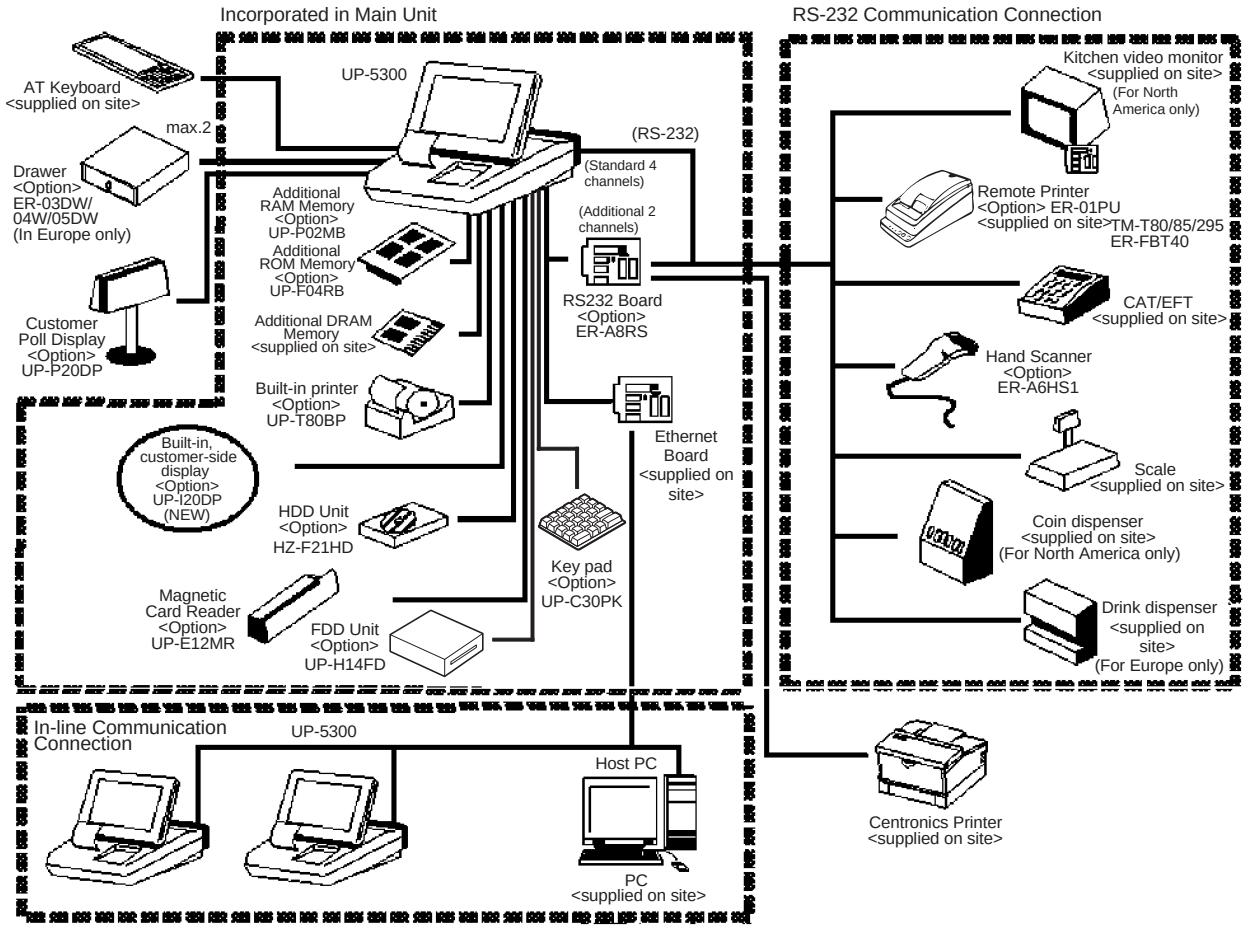
Please copy contents of FD provided from department to development PC. Install to UP-5300 by using APL Install Program from PC.

4-3. Memory map



CHAPTER 2. OPTIONS

1. System configuration



2. Options

No.	NAME	MODEL NAME	DESCRRIPTION
1	Expansion RAM disk board	UP-P02MB	2 Mbytes RAM board
2	Expansion ROM disk board	UP-F04RB	4 Mbytes ROM board
3	Customer display	UP-I20DP	2 line 20 digits dot display
4	Customer pole display	UP-P20DP	2 line 20 digits dot display
5	MCR (Magnetic Card Reader)	UP-E12MR2	for ISO 1 & 2 stripe card
6	Remote drawer	ER-03DW	7B/5C
		ER-04DW	5B/5C
		ER-05DW	5B/8C
7	Receipt/Journal printer	ER-01PU	2 station (R/J) thermal printer 45mm width
8	Built-in printer	UP-T80BP	1 station thermal printer 80mm width
9	RS232 & CENTRO I/F board	ER-A8RS	RS232 9 pins connector:2 ports Centronics 25 pins connector : 1 port
10	Hand scanner	ER-A6HS1	for reading bar code
11	FDD unit	UP-H14FD	3.5" Floppy Disk Drive (Newtronics D353M3)
12	Key pad	UP-C30PK	Std. 27 keys, Max. 30 keys
13	Key kit (Used for UP-C30PK)	ER-11KT7	1 × 1 key top kit
		ER-12KT7	1 × 2 key top kit
		ER-22KT7	2 × 2 key top kit
14	HDD unit	HZ-F21HD	2.1 GB HDD unit

3. Locally supplied options

No.	NAME	MODEL NAME	DESCRIPTION	
1	S.O.DIMM		Small Outline DIMM	Max. 32Mbyte * 1
2	PC keyboard		PS/2 type PC keyboard	
3	Application software			
4	Additional device drivers			

* 1 EXTENSION RAM MODULE (Provided through SHARP Electronics Corporation)

[Outline] UP-5300 has a socket as Small Outline DIMM.
It is necessary to satisfy with S.O.DIMM memory specification as follows.

[Specification]

	144pin S.O.DIMM		
	8 Mbytes	16 Mbytes	32 Mbytes
TYPE	EDO type		
ACCESS TIME	60 nsec. (less than)		
POWER	3.3 V		
REFRESH CYCLE	1024/16 msec.	2048/32 msec.	4096/64 msec.
REFRESH TYPE	CBR		
POWER CONSUMPTION	700 mA (less than)		
OTHER	4 chip × 16 Mbits (1 Mwords × 16 bits)	8 chip × 16 Mbits (2 Mwords × 8 bits)	4 chip × 64 Mbits (4 Mwords × 16 bits)

4. Service options

No.	NAME	PARTS CODE	PRICE	DESCRIPTION
1	Connector cable for Dongle (LPT-1)	QCNW-7858BHZZ	BL	Relay line from Terminal to Dongle
2	HDD mounting kit (For KB version)	DKIT-8671RCZZ	—	Bracked assembly for mounting
3	1 hole clerk key The key No.1 to No.6 ore supplied together with UP-5300.	LKGIM1004BH07	BH	Key No.7
		LKGIM1004BH08	BH	Key No.8
		LKGIM1004BH09	BH	Key No.9
		LKGIM1004BH10	BH	Key No.10
		LKGIM1004BH11	BH	Key No.11
		LKGIM1004BH12	BH	Key No.12
		LKGIM1004BH13	BH	Key No.13
		LKGIM1004BH14	BH	Key No.14
		LKGIM1004BH15	BH	Key No.15
		LKGIM1004BH16	BH	Key No.16
		LKGIM1004BH17	BH	Key No.17
		LKGIM1004BH18	BH	Key No.18
		LKGIM1004BH19	BH	Key No.19
		LKGIM1004BH20	BH	Key No.20
		LKGIM1004BH21	BH	Key No.21
		LKGIM1004BH22	BH	Key No.22
		LKGIM1004BH23	BH	Key No.23
		LKGIM1004BH24	BH	Key No.24
		LKGIM1004BH25	BH	Key No.25
		LKGIM1004BH26	BH	Key No.26
		LKGIM1004BH27	BH	Key No.27
		LKGIM1004BH28	BH	Key No.28
		LKGIM1004BH29	BH	Key No.29
		LKGIM1004BH30	BH	Key No.30
		LKGIM1004BH31	BH	Key No.31
		LKGIM1004BH32	BH	Key No.32
		LKGIM1004BH33	BH	Key No.33
		LKGIM1004BH34	BH	Key No.34
		LKGIM1004BH35	BH	Key No.35
		LKGIM1004BH36	BH	Key No.36
		LKGIM1004BH37	BH	Key No.37

No.	NAME	PARTS CODE	PRICE	DESCRIPTION
3	1 hole clerk key The key No.1 to No.6 ore supplied together with UP-5300.	L K G I M1 0 0 4 B H3 8	BH	Key No.38
		L K G I M1 0 0 4 B H3 9	BH	Key No.39
		L K G I M1 0 0 4 B H4 0	BH	Key No.40
		L K G I M1 0 0 4 B H4 1	BH	Key No.41
		L K G I M1 0 0 4 B H4 2	BH	Key No.42
		L K G I M1 0 0 4 B H4 3	BH	Key No.43
		L K G I M1 0 0 4 B H4 4	BH	Key No.44
		L K G I M1 0 0 4 B H4 5	BH	Key No.45
		L K G I M1 0 0 4 B H4 6	BH	Key No.46
		L K G I M1 0 0 4 B H4 7	BH	Key No.47
		L K G I M1 0 0 4 B H4 8	BH	Key No.48
		L K G I M1 0 0 4 B H4 9	BH	Key No.49
		L K G I M1 0 0 4 B H5 0	BH	Key No.50
		L K G I M1 0 0 4 B H5 1	BH	Key No.51
		L K G I M1 0 0 4 B H5 2	BH	Key No.52
		L K G I M1 0 0 4 B H5 3	BH	Key No.53
		L K G I M1 0 0 4 B H5 4	BH	Key No.54
		L K G I M1 0 0 4 B H5 5	BH	Key No.55
		L K G I M1 0 0 4 B H5 6	BH	Key No.56
		L K G I M1 0 0 4 B H5 7	BH	Key No.57
		L K G I M1 0 0 4 B H5 8	BH	Key No.58
		L K G I M1 0 0 4 B H5 9	BH	Key No.59
		L K G I M1 0 0 4 B H6 0	BH	Key No.60
		L K G I M1 0 0 4 B H6 1	BH	Key No.61
		L K G I M1 0 0 4 B H6 2	BH	Key No.62
		L K G I M1 0 0 4 B H6 3	BH	Key No.63
		L K G I M1 0 0 4 B H6 4	BH	Key No.64
		L K G I M1 0 0 4 B H6 5	BH	Key No.65
		L K G I M1 0 0 4 B H6 6	BH	Key No.66
		L K G I M1 0 0 4 B H6 7	BH	Key No.67
		L K G I M1 0 0 4 B H6 8	BH	Key No.68
		L K G I M1 0 0 4 B H6 9	BH	Key No.69
		L K G I M1 0 0 4 B H7 0	BH	Key No.70
		L K G I M1 0 0 4 B H7 1	BH	Key No.71
		L K G I M1 0 0 4 B H7 2	BH	Key No.72
		L K G I M1 0 0 4 B H7 3	BH	Key No.73
		L K G I M1 0 0 4 B H7 4	BH	Key No.74
		L K G I M1 0 0 4 B H7 5	BH	Key No.75
		L K G I M1 0 0 4 B H7 6	BH	Key No.76
		L K G I M1 0 0 4 B H7 7	BH	Key No.77
		L K G I M1 0 0 4 B H7 8	BH	Key No.78
		L K G I M1 0 0 4 B H7 9	BH	Key No.79
		L K G I M1 0 0 4 B H8 0	BH	Key No.80
		L K G I M1 0 0 4 B H8 1	BH	Key No.81
		L K G I M1 0 0 4 B H8 2	BH	Key No.82
		L K G I M1 0 0 4 B H8 3	BH	Key No.83
		L K G I M1 0 0 4 B H8 4	BH	Key No.84
		L K G I M1 0 0 4 B H8 5	BH	Key No.85
		L K G I M1 0 0 4 B H8 6	BH	Key No.86
		L K G I M1 0 0 4 B H8 7	BH	Key No.87
		L K G I M1 0 0 4 B H8 8	BH	Key No.88
		L K G I M1 0 0 4 B H8 9	BH	Key No.89
		L K G I M1 0 0 4 B H9 0	BH	Key No.90
		L K G I M1 0 0 4 B H9 1	BH	Key No.91
		L K G I M1 0 0 4 B H9 2	BH	Key No.92
		L K G I M1 0 0 4 B H9 3	BH	Key No.93

No.	NAME	PARTS CODE	PRICE	DESCRIPTION
3	1 hole clerk key The key No.1 to No.6 ore supplied together with UP-5300.	LKGI M1004BH94	BH	Key No.94
		LKGI M1004BH95	BH	Key No.95
		LKGI M1004BH96	BH	Key No.96
		LKGI M1004BH97	BH	Key No.97
		LKGI M1004BH98	BH	Key No.98
		LKGI M1004BH99	BH	Key No.99
		LKGI M1004BH00	BH	Key No.100
		LKGI M1004BHA1	BH	Key No.101
		LKGI M1004BHA2	BH	Key No.102
		LKGI M1004BHA3	BH	Key No.103
		LKGI M1004BHA4	BH	Key No.104
		LKGI M1004BHA5	BH	Key No.105
		LKGI M1004BHA6	BH	Key No.106
		LKGI M1004BHA7	BH	Key No.107
		LKGI M1004BHA8	BH	Key No.108
		LKGI M1004BHA9	BH	Key No.109
		LKGI M1004BHA0	BH	Key No.110
		LKGI M1004BHB1	BH	Key No.111
		LKGI M1004BHB2	BH	Key No.112
		LKGI M1004BHB3	BH	Key No.113
		LKGI M1004BHB4	BH	Key No.114
		LKGI M1004BHB5	BH	Key No.115
		LKGI M1004BHB6	BH	Key No.116
		LKGI M1004BHB7	BH	Key No.117
		LKGI M1004BHB8	BH	Key No.118
		LKGI M1004BHB9	BH	Key No.119
		LKGI M1004BHB0	BH	Key No.120
		LKGI M1004BHC1	BH	Key No.121
		LKGI M1004BHC2	BH	Key No.122
		LKGI M1004BHC3	BH	Key No.123
		LKGI M1004BHC4	BH	Key No.124
		LKGI M1004BHC5	BH	Key No.125
		LKGI M1004BHC6	BH	Key No.126

5. Service tools

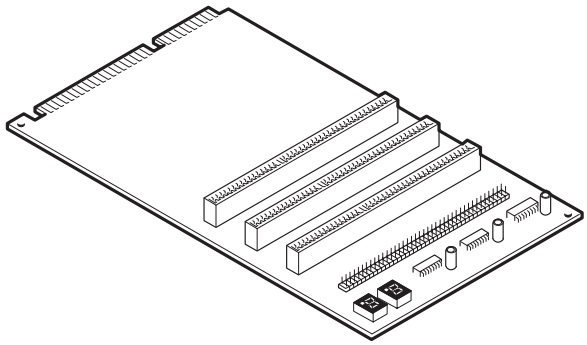
No.	NAME	PARTS CODE	PRICE	DESCRIPTION
1	Service tool kit	DKIT-8656BHZZ	CW	ISA checker ISA relay board
2	Printer connector signal loop back connector	UKOG-6717RCZZ	BR	for ER-A8RS CENTRONICS connector
3	MCR test card	UKOG-6718RCZZ	BE	for UP-E12MR
4	RS232 loop back connector	UKOG-6705RCZZ	BC	for RS232 connector
5	CPU/VGA PWB relay PWB	CKOG-6728BHZZ	CQ	
6	BIOS loading board	CKOG-6727BHZZ	CS	for overwriting BIOS
7	RS232 modular jack loop back connector	UKOG-6729BHZZ	AZ	for RJ45 connector
8	BIOS MASTER ROM	VHI27040RBQ1B	—	EP-ROM for overwriting BIOS
9	TOUCH PEN	CPENP1004PCN5	AG	

4-1. Service tool kit: DKIT-8656BHZZ

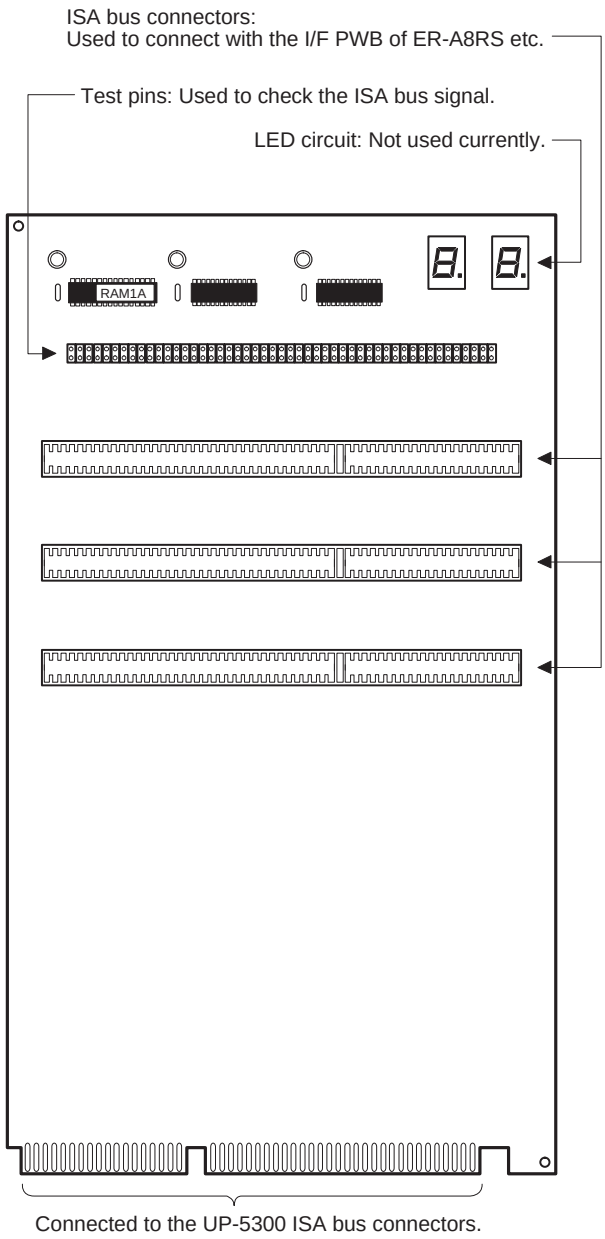
1) ISA checker

Used to repair or check the operation of the optional I/F.

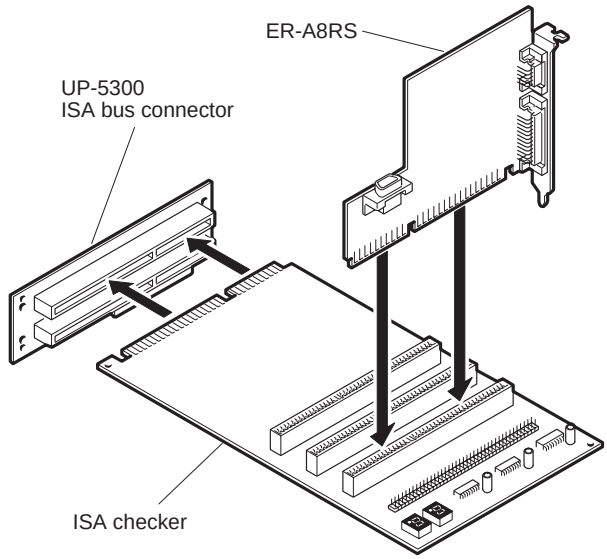
- External view



- Plain view


ISA bus connectors:
Used to connect with the I/F PWB of ER-A8RS etc.
Test pins: Used to check the ISA bus signal.
LED circuit: Not used currently.
RAM1A
Connected to the UP-5300 ISA bus connectors.

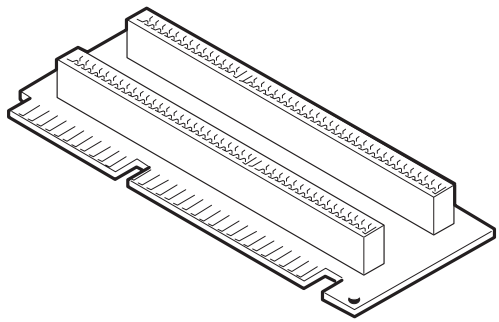
- Connection diagram



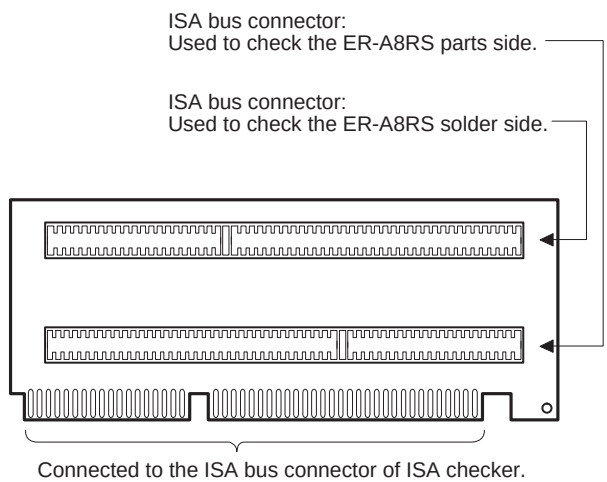
2) ISA relay board

Connected to the ISA checker for installation of the optional I/F horizontally and for repairing and checking the operation .

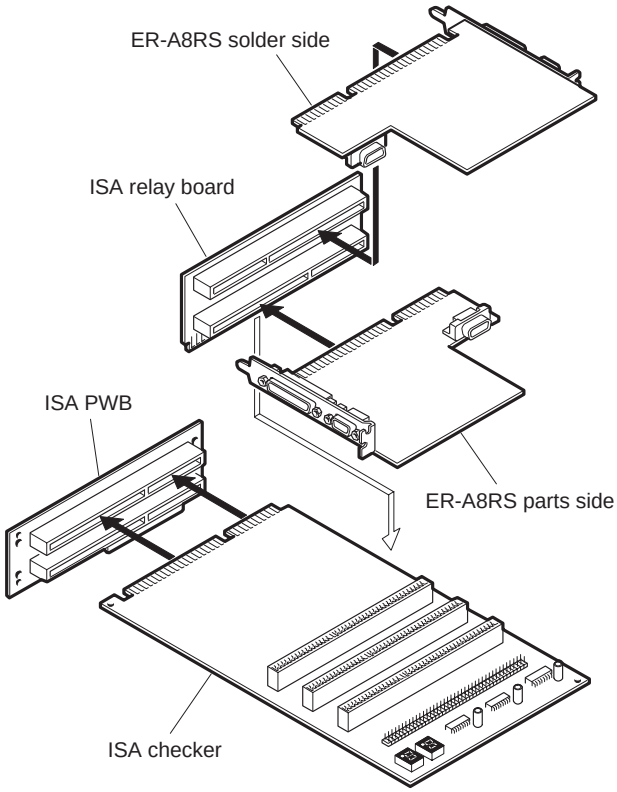
- External view



- Plain view


ISA bus connector:
Used to check the ER-A8RS parts side.
ISA bus connector:
Used to check the ER-A8RS solder side.
Connected to the ISA bus connector of ISA checker.

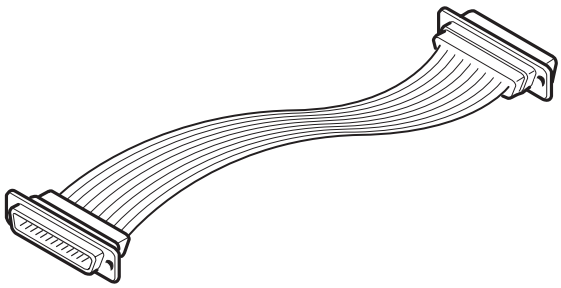
- Connection diagram



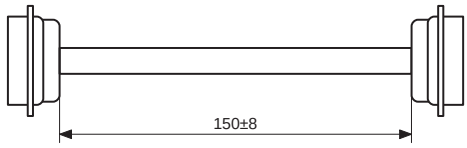
4-2. Printer connector signal loop check cable: UKOG-6717RCZZ

Connected to the centronics connector (25 pin) of the ER-A8RS, and is used to check loop signals when executing diagnostics.

- External view

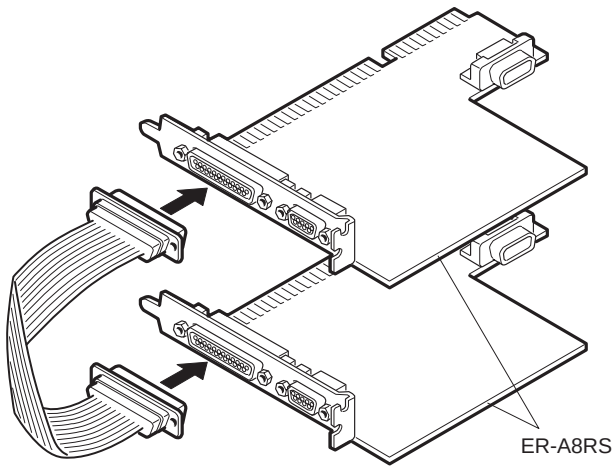


- Plan view and connection diagram



Signal name	Pin No.		Pin No.	Signal name
STROBE-	1		1	STROBE-
DB0	2		2	DB0
DB1	3		3	DB1
DB2	4		4	DB2
DB3	5		5	DB3
DB4	6		6	DB4
DB5	7		7	DB5
DB6	8		8	DB6
DB7	9		9	DB7
ACK-	10		10	ACK-
BUSY	11		11	BUSY
PE	12		12	PE
SLCT	13		13	SLCT
AUTOFD-	14		14	AUTOFD-
ERROR-	15		15	ERROR-
INIT-	16		16	INIT-
SLCTIN-	17		17	SLCTIN-
PE	18~25		18~25	PE

- Connection diagram



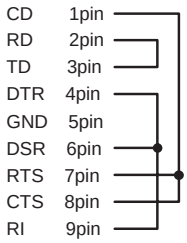
4-3. MCR test card: UKOG-6718RCZZ

- Used when executing the diagnostics of the UP-E12MR2.
- External view

4-4. RS232 loop back connector: UKOG-6705RCZZ

Connected to the RS232 connector (D-SUB 9 pin: COM1, COM2, COM3, COM4) of the UP-5300 and ER-A8RS, and used to check loop signals when executing diagnostics.

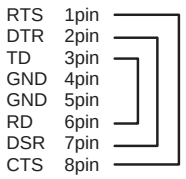
- Connection diagram



4-5. RS232 modular jack loop back connector: UKOG-6729BHZZ

Connected to the RS232 connector (RJ45: COM3, COM4, COM5, COM6) of the UP-5300, and used to check loop signals when executing diagnostics.

- Connection diagram



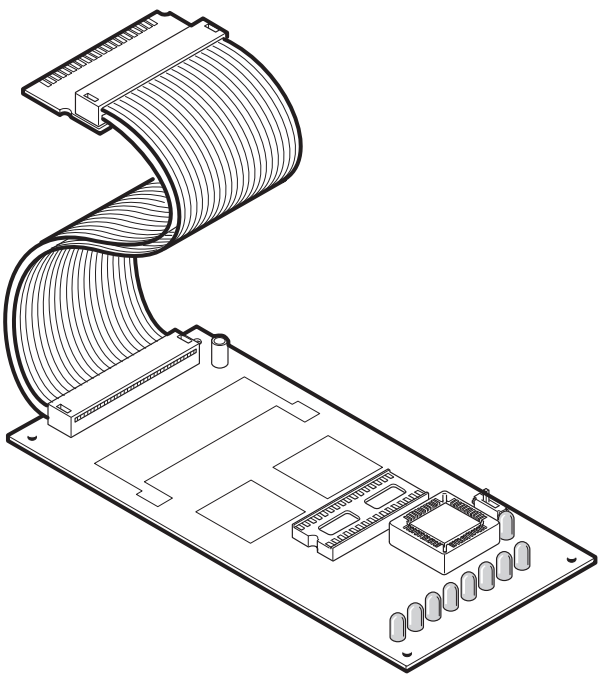
4-6. BIOS loading board: CKOG-6727BHZZ

The BIOS loading board: CKOG-6727BHZZ is a tool to write a BIOS ROM program in the F-ROM on the UP-5300's main board. Use this PWB in the following cases:

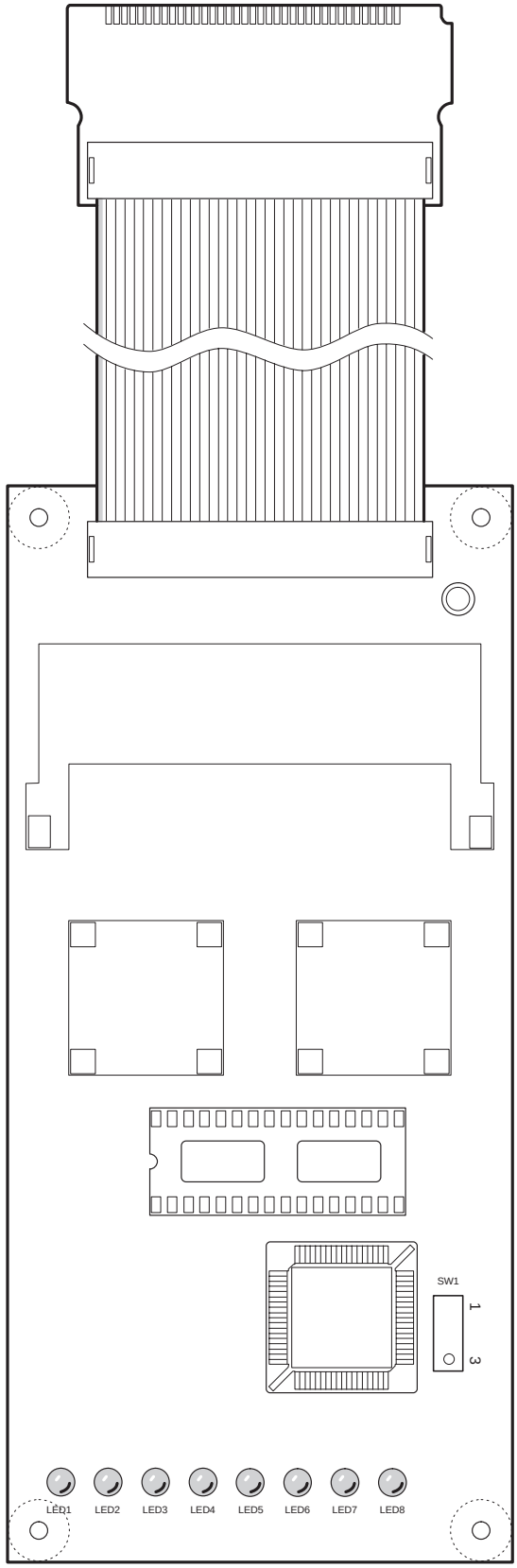
- The F-ROM on the UP-5300's main board be comes unreadible and a BIOS ROM program must be written in the F-ROM.
- The BIOS ROM program in the F-ROM is overwritten due to the version up of BIOS ROM program, etc.

The BIOS loading board is connected to the Option ROM/RAM disk connector (CN5) of the Main PWB.

- External view



- Plain view

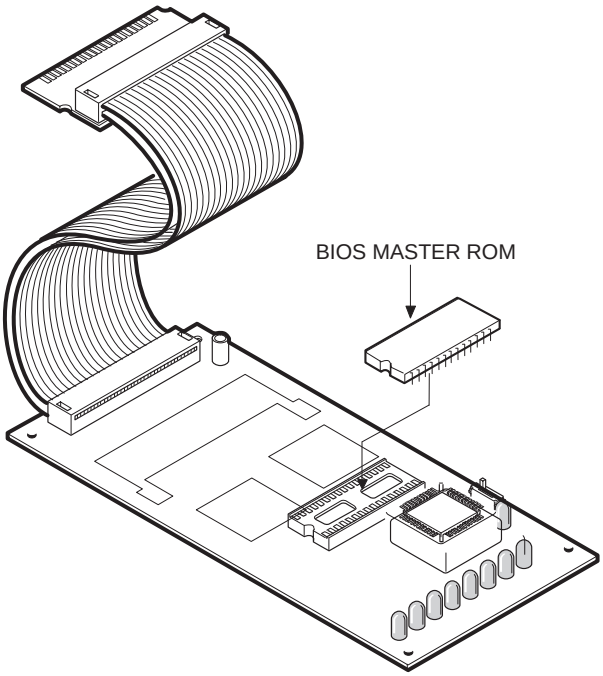


- Connection diagram

Writing BIOS ROM Program

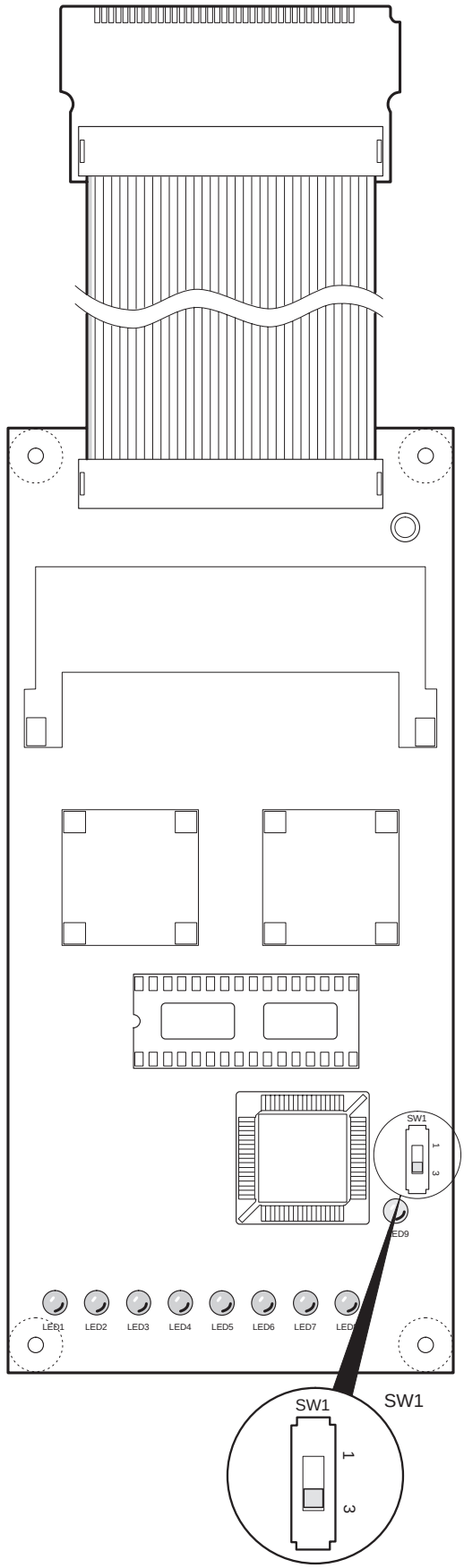
NOTE: Remove all option boards from the ISA slots before writing on the BIOS ROM.

1. Install the EP-ROM (master ROM): containing a BIOS program on the BIOS loading board: CKOG-6727RCZZ.

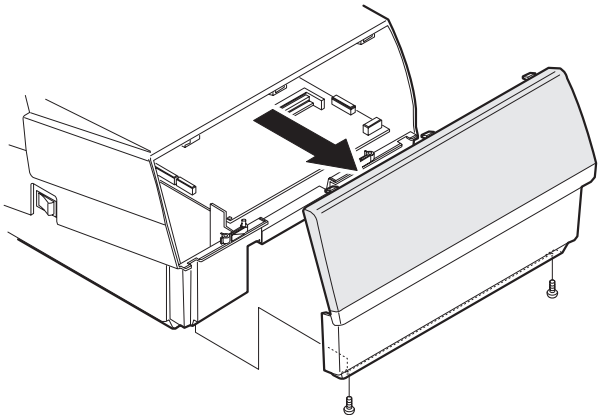


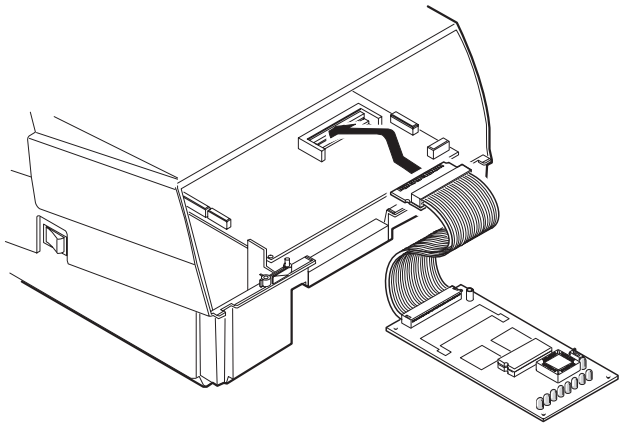
∗ Caution: The AC power must be removed prior to installing the BIOS loading board.

2. Set SW1 on the BIOS loading board to the side of pin 3.



3. Open the upper cabinet.
4. Connect the BIOS loading board to the option ROM/RAM connector CN5 on the main PWB, and then close the cabinet.





5. Writing the BIOS ROM program starts by turning on the power switch on the right side.

   To determine the status of the LED lights on the special service PWB when a BIOS ROM program is being written, see the table on the next page.

   Writing is complete (automatic completion) when the green LED (LED9) on the BIOS loading board lights up.
6. After writing is complete, turn off the power switch on the right side to remove the BIOS loading board, and turn on the power switch on the left side again to check whether the BIOS program starts up normally or not.

LED DISPLAY STATUS

[◎ : ON (Lighting) — : OFF]

<In normal operation>

LED1 (RED)	LED2 (RED)	LED3 (RED)	LED4 (RED)	LED5 (RED)	LED6 (RED)	LED7 (RED)	LED8 (RED)	LED9 (GREEN)	FUNCTION
◎	◎	◎	◎	◎	◎	◎	◎	—	Start of COPY FUNCTION
—	—	—	—	◎	—	—	—	—	Start initializing
—	—	—	—	—	◎	—	—	—	Erasing F-ROM (LED6: RED is blinking)
—	—	—	—	◎	◎	—	—	—	Start copy programming to F-ROM from EP-ROM
—	—	—	—	◎	◎	—	—	—	Programming: Bank0 C0000 h (64KB)
◎	—	—	—	◎	◎	—	—	—	Programming: Bank0 D0000 h (64KB)
—	◎	—	—	◎	◎	—	—	—	Programming: Bank0 E0000 h (64KB)
◎	◎	—	—	◎	◎	—	—	—	Programming: Bank0 F0000 h (64KB)
—	—	—	◎	◎	◎	—	—	—	Programming: Bank1 C0000 h (64KB)
◎	—	—	◎	◎	◎	—	—	—	Programming: Bank1 D0000 h (64KB)
—	◎	—	◎	◎	◎	—	—	—	Programming: Bank1 E0000 h (64KB)
◎	◎	—	◎	◎	◎	—	—	—	Programming: Bank1 F0000 h (64KB)
—	—	—	—	—	—	◎	—	—	Start verifying the program in the F-ROM
—	—	—	—	—	—	◎	—	—	Verifying: Bank0 C0000 h (64KB)
◎	—	—	—	—	—	◎	—	—	Verifying: Bank0 D0000 h (64KB)
—	◎	—	—	—	—	◎	—	—	Verifying: Bank0 E0000 h (64KB)
◎	◎	—	—	—	—	◎	—	—	Verifying: Bank0 F0000 h (64KB)
—	—	—	◎	—	—	◎	—	—	Verifying: Bank1 C0000 h (64KB)
◎	—	—	◎	—	—	◎	—	—	Verifying: Bank1 D0000 h (64KB)
—	◎	—	◎	—	—	◎	—	—	Verifying: Bank1 E0000 h (64KB)
◎	◎	—	◎	—	—	◎	—	—	Verifying: Bank1 F0000 h (64KB)
—	—	—	—	◎	—	◎	—	—	Setting protection the F-ROM
◎	◎	◎	◎	◎	◎	◎	◎	◎	END of complete COPY FUNCTION

<Erase ERROR in F-ROM>

LED1 (RED)	LED2 (RED)	LED3 (RED)	LED4 (RED)	LED5 (RED)	LED6 (RED)	LED7 (RED)	LED8 (RED)	LED9 (GREEN)	FUNCTION
◎	—	—	—	—	◎	—	◎	—	Device not ready
—	◎	—	—	—	◎	—	◎	—	VPP error
◎	◎	—	—	—	◎	—	◎	—	Command sequence error
—	—	◎	—	—	◎	—	◎	—	

<Programming ERROR in F-ROM>

LED1 (RED)	LED2 (RED)	LED3 (RED)	LED4 (RED)	LED5 (RED)	LED6 (RED)	LED7 (RED)	LED8 (RED)	LED9 (GREEN)	FUNCTION
◎	—	—	—	◎	◎	—	◎	—	Device not ready
—	◎	—	—	◎	◎	—	◎	—	VPP error
◎	◎	—	—	◎	◎	—	◎	—	Command sequence error

<Verifying ERROR in F-ROM>

LED1 (RED)	LED2 (RED)	LED3 (RED)	LED4 (RED)	LED5 (RED)	LED6 (RED)	LED7 (RED)	LED8 (RED)	LED9 (GREEN)	FUNCTION
◎	—	—	—	◎	—	◎	◎	—	Device not ready while release the protection
—	◎	—	—	◎	—	◎	◎	—	Can not release the protection

CHAPTER 3. SERVICE PRECAUTION

1. Conditions for soldering circuit parts

To solder the following parts manually, follow the conditions described below.

PARTS NAME	PARTS CODE	LOCATION	CONDITIONS FOR SOLDERING
Ceramic oscillator	RCRMZ7002RCZZ	TOCH PANEL CONTROL PWB: X1 (8M)	270°C/3sec.
	RCRMZ7003RCZZ	MAIN PWB: X2 (24M)	
	RCRMZ7004RCZZ	MAIN PWB: X2 (7.37M)	
DIP SWITCH	QSW-Z7011XCZZ	SWITCH PWB: S2	300°C/3sec.

2. Cautions on handling CPU and POWER FAN

When removing or performing maintenance activities on the CPU and POWER FAN, be sure to handle them with care, because it may cause abnormal sounds or deteriorate their performance if they are dropped or exposed to a heavy impact.

3. Note for handling of Touch panel

- The transparency of the touch panel should be vitally important. Use clean gloves and masks.
- For handling, do not hold the transparent area, and do not hold the heat seal connector section to assure reliability.
- Do not overlay touch panels. The edge may damage the surface.
- Do not place heavy things on the touch panel.
- Do not apply a strong shock, and do not drop it.
- When attaching the protection film again, carefully check for dirt. If there is any dirt, it is transferred.
- To clean dirt on the surface, use a dry, soft cloth or a cloth immersed in ethyl alcohol.
- Check that the housing does not give stress to the touch panel.
- Be careful not to touch the touch panel with tools.
- The heat seal section is easily disconnected. Be careful not to place stress to the heat seal section when installing.
- The touch panel is provided with an air groove to make the external and the internal air pressure equal to each other. If water or oil is put around the air groove, it may penetrate inside. Be careful to keep the air groove away from water and oil.
- Do not use SHARP objects when making input entrres.

4. Note for handling of LCD

- The LCD elements are made of glass. BE careful not to expose them strong mechanical shock, or they may be broken. Use extreme care not to break them.
- If the LCD element is broken and the liquid leaks, avoid contact with your mouth or eyes. If the liquid comes in contact with your skin or clothes, immediately clean with soap.
- Use the unit under the rated conditions to prevent against damage.
- Be careful not to place water or other liquids on the display surface.
- The reflection plate and the polarizing plate are easily scratched. BE careful not to touch them with a hard object such as glass, tweezers etc. Never hit, push, or rub the surface with hard objects.
- When installing the unit, be careful not to apply stress to the LCD module. If excessive stress is applied, abnormal display or uneven color may result.

5. Cautions on handling connectors

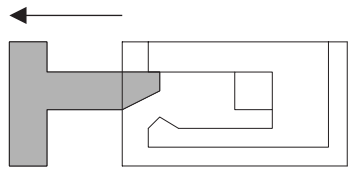
When connecting or disconnecting the following connectors, follow the procedures below.

1)

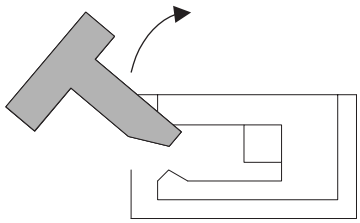
PARTS NAME	PARTS CODE	LOCATION
FFC CONNECTOR	QCNCW2812BH3J	LCD RELAY PWB: CN8

- **How to insert FFC**

(1) Pull the slider to the unlock position.

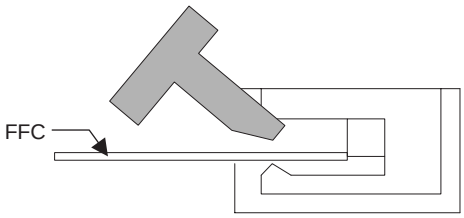


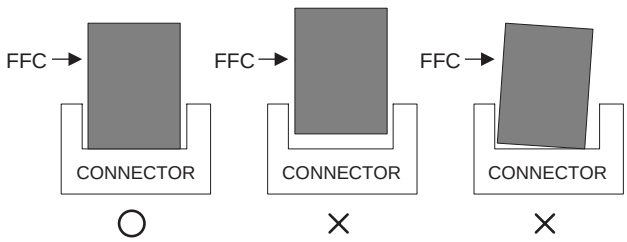
(2) Open the slider upwards.



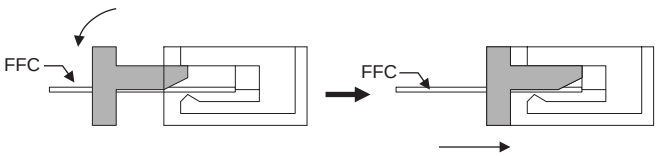
(3) Inserting the FFC

Insert the FFC firmly until the FFC hits the bottom of the connector's insulator.





(4) Close the slider to the lock position



6. AT Keyboard usable for UP-5300

The UP-5300 can be externally connected to a keyboard.
The UP-5300's key BIOS conforms to the PC standard, but this BIOS's operation is not compatible for some keyboards.
Some keyboards may cause operation errors due to delicate timing and conflicts.
It is currently found that the following models of keyboards may malfunction.
When selecting a keyboard to be connected, test the keyboard in advance to check that it correctly works.

- Japanese keyboard (106 keys)
  Manufactured by IBM: TYPE/MODEL5576-B01 FRUPN66G0507
- English keyboard (101 keys)
  Manufactured by NMB Technologies Inc.: Model: RT6651T+

CHAPTER 4. UP-5300 DIAGNOSTICS SPECIFICATIONS

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      1) Key Pad Check 4-18

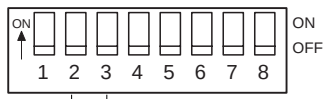
Subsequently the POS application software is added which may over-write the F-ROM area.

Please check to insure that the diagnostic program is installed along with the POS application.

Starting Diagnostics when an Application software is installed:

(1) Execute the diagnostic program by rebooting the UP-5300 from the BIOS-ROM (MASK ROM).

1) Remove AC power by placing the power switch to the "off" position.
2) Set the system switches (DSW-2 and DSW-3) as follows:



DSW-3

Function	OFF (value = 1)	ON (value = 0)
Boot Drive	Drive A:	Drive C:

DSW-2

Function	OFF (value = 1)	ON (value = 0)
Drive A: Device	Mask ROM	FDD

3) Connect the AT keyboard.
4) Turn on the AC power on to start upthe BIOS-ROM (MASK ROM).
   Then the incorporated system installer utility will start.
5) Press the ESC key on the AT keyboard, and select "EXIT" followed by pressing the ENTER key to exit the System installer.
   The UP-5300 will go to the A:\> prompt.
6) To select the drive that of diagnostics program, type "C:\" followed by the ENTER key.
7) At the "C:\" prompt , type "SRV" followed by the ENTER key to start the serviceman's diagnostic program.

Starting Diagnostics when an Application software is installed:

(2) To execute the diagnostic program when an application program is also installed.

1) Remove AC power by placing the power switch to the "off" position.
2) Set the system switches (DSW-2 and DSW-3) as shown above:
3) Connect the AT keyboard.
4) Turn on the AC power.

5) Depress the F8 function key located on the AT keyboard and start the UP-5300 without executing the "CONFIG.SYS" and the "AUTOEXEC.BAT". The UP-5300 will go to the A:\> prompt.
6) To select the drive that of diagnostics program, type "C:\" followed by the ENTER key.
7) At the "C:\" prompt , type "SRV" followed by the ENTER key to start the serviceman's diagnostic program.

1. General

This diagnostic program is used to check the PWB's, the process, and the machine of UP-5300 series in a simplified manner.

This test program is supplied with floppy disks.

2. System configuration

The system requires the UP-5300, and an AT keyboard for diagnostic operations.

3. Service diagnostics

3-1. Service diagnostics getting started

Getting started:

Execute "SRV.BAT" by entering the command with the AT keyboard as follows:

C:\> SRV ↵

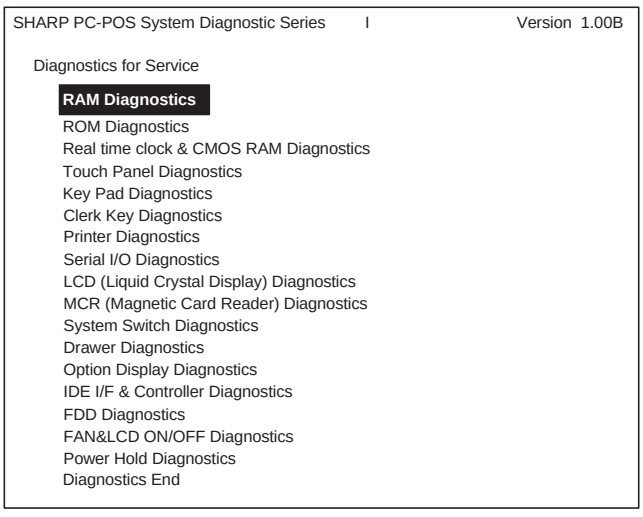
"C:\>" is the DOS prompt. (Used by the F-ROM disk based on the settings of the system switches.)

∗ Do not load any device drivers when using this program.

∗ To operate other applications after performing this program, reboot the machine.

3-2. Selection menu

The diagnostics menu is started and the following menu is displayed. The highlighted cursor is moved by the cursor keys (UP ↑ and DOWN ↓) of the AT keyboard. Move the cursor to the desired item, and press the Enter key to execute the selected diagnostics program. When the selected diagnostics program is completed, the display returns to the menu screen by pressing the ESC key. Select "Diagnostics End" and press the Enter key to terminate the diagnostics.



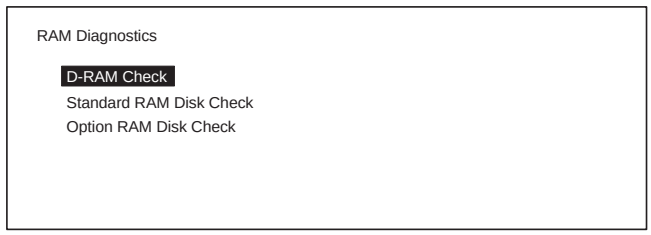
3-3. RAM Diagnostics

This program is used to test the standard memory, the extension memory, and the RAM disk.

When this program is selected, the following menu is displayed.

The highlighted cursor is moved by the cursor keys (UP ↑ and DOWN ↓) of the AT keyboard. Move the cursor to the desired item, and press the Enter key to execute the selected diagnostics program.

When the selected diagnostics program is completed, Press the ESC key to return to the RAM menu screen. Pressing the Esc key again returns to the service diagnostics menu.



1) D-RAM Check

① Checking content

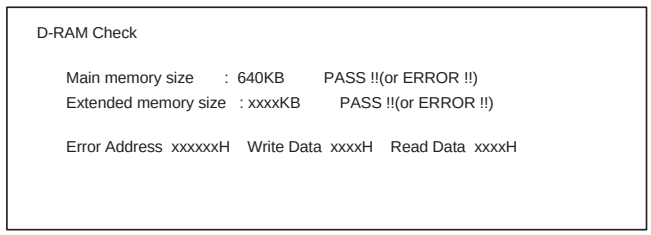
All memory areas are checked in units of 64KB. The checking procedures are as follows:

i. Test data 5555H is written to all the test areas.
ii. Test data and read data are compared by each word, If it is O.K., test data AAAAH is written to the test area.
iii. Test data and read data are compared by each word, If it is O.K., test data 5555H is written to the test area.
iv. Test data 0000H is written to all the test areas.
v. Test data and read data are compared by each word, If it is O.K., test data FFFFH is written to the test area.
vi. Test data and read data are compared by each word, If it is O.K., test data 0000H is written to the test area.

When an error occurs during the test, the error address and data are displayed and the test is stopped.

For the extension memory test, the value set in the setup of read and test and is made to the area in increments of 64KB.

② Display


D-RAM Check
Main memory size : 640KB PASS !!(or ERROR !!)
Extended memory size : xxxxKB PASS !!(or ERROR !!)
Error Address xxxxxxH Write Data xxxxH Read Data xxxxH

When testing the extension memory size, the value set in the setup is displayed. The error address and the error data are displayed only when an error occurs. (When no errors occur, they are not displayed.)

③ Terminating method

After completion of the test, press Esc key to terminate the test to return to the RAM diagnostics menu.

2) Standard RAM Disk Check

① Checking content

When testing the standard RAM disk area (BANK 000H ~ 03FH), each test area of bank size 16KB is checked. The bank base address of RAM is set to 0D4000H and after. The checking procedures are as follows:

i. Write different data to the following address by word method. After the completion of writing, a BANK 03FH 0D4000H data read verify check is made. (Data in the written area is saved in the main memory.) If it is OK, the following test is executed. In case of an error, the error display is made and the test is terminated.

Write address	Write data
BANK BFH (extension) 0D4000H	BF40H
BANK 7FH (extension) 0D4000H	7F80H
BANK 3FH (standard) 0D4000H	3FC0H

ii. The test area data is saved to the main memory.
iii. Test data 5555H is written to all the test areas.
iv. Test data and read data are compared by each word, If it is O.K., test data AAAAH is written to the test area.
v. Test data and read data are compared by each word, If it is O.K., test data 5555H is written to the test area.
vi. Test data 0000H is written to all the test areas.
vii. Test data and read data are compared by each word, If it is O.K., test data FFFFH is written to the test area.
viii. Test data and read data are compared by each word, If it is O.K., test data 0000H are written to the test area.
ix. The saved data is written to the test areas.

When an error occurs during the test, the error address and data are displayed and the test is stopped.

② Display

```
Standard RAM Disk Check

    Standard RAM Disk size : 1024KB      PASS !!(or ERROR !!)

    Error Address  xxxxxxH   Write Data  xxxxH   Read Data  xxxxH
```

The error address and the error data are displayed only when an error occurs. (If no errors occur, they are not displayed.)

③ Terminating method

After the test result is displayed, press the Esc key to terminate the test and return to the RAM diagnostics menu.

3) OPTION RAM Disk Check

① Checking content

For the standard RAM disk area (BANK 040H ~ BANK 0BFH), each test area of bank size 16KB is checked. The bank base address of RAM is set to 0D4000H and after. The check procedures are as follows:

i. Write different data to each address by a word method similar to the Standard RAM Disk Check. After completion of writing, a BANK 0BFH 0D4000H data read verify check is made. (Data in the written area is saved in the main memory.) If it is OK, the following test is executed. In case of an error, the error display is made and the test is terminated.
ii. Test data 55AAH is written to BANK 040H 0D4000H.
iii. BANK 040H 0D4000H is read and compared with 55AAH. If both data are correct, the following test is executed. If not, "Extended RAM Disk size: 0KB" is displayed and the test is terminated.
iv. The test area data is saved to the main memory.
v. Test data 5555H is written to the test area.
vi. Test data and read data are compared. If is OK, test data AAAAH is written to the test area.
vii. Test data and read data are compared by each word, If it is O.K., test data 5555H is written to the test area.
viii. Test data and read data are compared by each word, If it is O.K., test data 0000H is written to all the test areas.
ix. Test data and read data are compared by each word. If it is OK, test data FFFFH is written to the test area.
x. Test data and read data are compared by each word. If it is OK, test data 0000H is written to the test area.
xi. The saved data is written to the test areas.

When an error occurs during the test, the error address and data are displayed and the test is stopped.

② Display

```
Option RAM disk Check

    Extended RAM Disk size : 1024KB      PASS !!(or ERROR !!)

    Error Address  xxxxxxH   Write Data  xxxxH   Read Data  xxxxH
```

The error address and the error data are displayed only when an error occurs. (If no error occurs, they are not displayed.)

③ Terminating method

After the test result is displayed, press the Esc key to terminate the test and return to the RAM diagnostics menu.

3-4. ROM Diagnostics

The DOS ROM, BIOS ROM, standard flash ROM, and option flash ROM are tested.

The following menu is displayed. The highlighted cursor is moved by the cursor keys (UP ↑ and DOWN ↓) of the AT keyboard. Move the cursor to the desired item, and press the Enter key to execute the selected diagnostics program. When the selected diagnostics program is completed, Press the ESC key to return to the ROM diagnostics menu. Pressing Esc key again returns to the service diagnostics menu.

```
ROM Diagnostics

    DOS ROM Check
    BIOS ROM Check
    Standard FLASH ROM Check
    Option FLASH ROM Check
```

1) DOS ROM Check

① Checking content

A sum check is made for the DOS ROM (BANK 000H ~ 0FFH). All data bytes are added. If the check sum is 10H, it is normal.

The ROM version is displayed.

② Display

```
DOS ROM Check

    Sum Check      :  PASS !!(or ERROR !!)
    ROM Version    :  VHILH****
                          ↑
                      The version is displayed.
```

③ Terminating method

After the test result is displayed, press the Esc key to terminate and return to the ROM diagnostics menu.

2) BIOS ROM Check

① Checking content

The BIOS ROM version is displayed.

② Display

```
BIOS ROM Check

    Version  -  ROM  :  SHPUP****
                          ↑
                      The version is displayed.
```

③ Terminating method

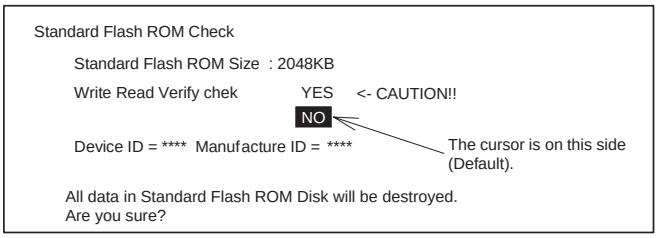
After the test result is displayed, press Esc key to terminate and return to the ROM diagnostics menu.

3) Standard FLASH ROM Check

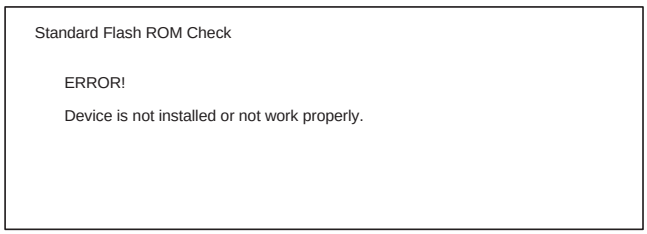
① Checking content

Write and read are performed to the standard FLASH ROM area (BANK 200H ~ 27FH) to establish a verify check. The check procedures is as follows:

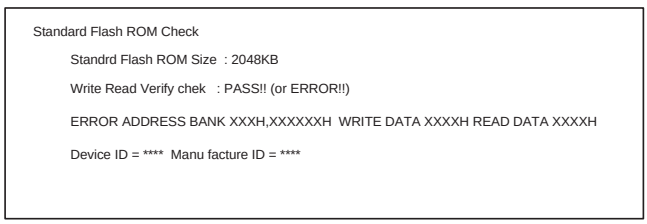
- The ID code, the manufacture, and the device signature code are read and displayed.
- The ROM size is specified and the following display is made to allow the user to select whether to perform the verify check or not.
- Move cursor to select "YES", and the message in ( ) will be displayed.
- If the verify check is made, the test area is first erased.
- Increment data for each byte is written to all the test areas.
- (Example: "0001h", "0202h", "0405h", --- "0E0Fh", --- "FEFFh" ∗ The two left digits are the lower address, and the two right address are the upper address.)
- Read verify check is performed.


Standard Flash ROM Check
Standard Flash ROM Size : 2048KB
Write Read Verify chek YES <- CAUTION!!
NO
Device ID = **** Manufacture ID = ****
The cursor is on this side (Default).
All data in Standard Flash ROM Disk will be destroyed.
Are you sure?

If the proper value is not read, the following display is made. (Press the ESC key to terminate the test.)



② Final display


Standard Flash ROM Check
Standrd Flash ROM Size : 2048KB
Write Read Verify chek : PASS!! (or ERROR!!)
ERROR ADDRESS BANK XXXH,XXXXXXH WRITE DATA XXXXH READ DATA XXXXH
Device ID = **** Manu facture ID = ****

③ Terminating method

After the test result is displayed, press the Esc key to terminate and return to the ROM diagnostics menu.

4) Option FLASH ROM Check

① Checking content

Write read verify check or read check is performed for the optional FLASH ROM area (BANK 280H – 3FFH). The checking procedure is as follows:

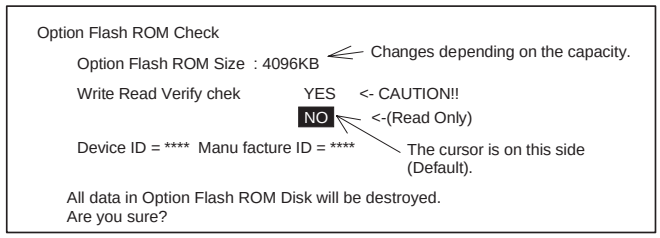
- The ID code, the manufacture, and the device signature code are read in BANK 280H ~ 2FFH, BANK 300H ~ 37FH, and BANK 380H ~ 3FFH to check that the proper value is read or not.
- If the proper value is read, the ROM size is specified and the following display is made to allow the user to select whether to perform the verify check or not.

When "YES" is selected

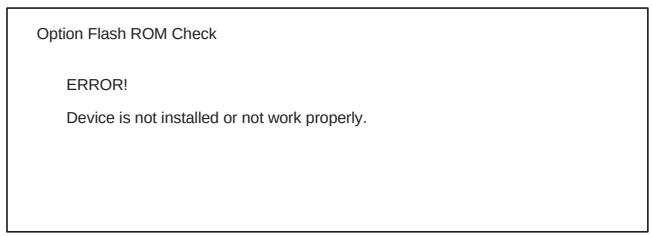
- Move cursor to select "YES", and the message in ( ) will be displayed.
- If the verify check is made, the test area is first erased.
- Increment data for each byte is written to all the test areas.
- (Example: "0001h", "0203h", "0405h", ··· "0E0Fh", ··· "FEFFh" ∗ The two left digits are the lower address, and the two right address are the upper address.)
- Read verify check is performed.

When "NO" is selected

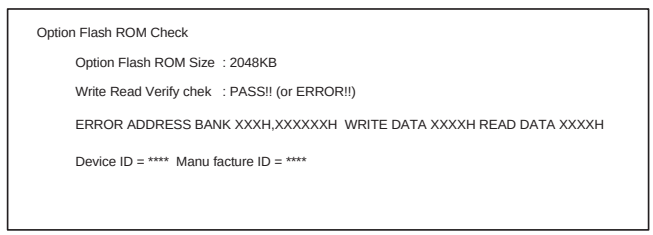
- When "NO" is selected, read check is performed for the above increment data. Therefore, the option FLASH ROM to be tested must be passed by write read verify check once.


Option Flash ROM Check
Option Flash ROM Size : 4096KB
Changes depending on the capacity.
Write Read Verify chek YES <- CAUTION!!
NO
<-(Read Only)
Device ID = **** Manu facture ID = ****
The cursor is on this side (Default).
All data in Option Flash ROM Disk will be destroyed.
Are you sure?

If the proper value is not read, the following display is made. (Press the ESC key to terminate the test.)



② Final display


Option Flash ROM Check
Option Flash ROM Size : 2048KB
Write Read Verify chek : PASS!! (or ERROR!!)
ERROR ADDRESS BANK XXXH,XXXXXXH WRITE DATA XXXXH READ DATA XXXXH
Device ID = **** Manu facture ID = ****

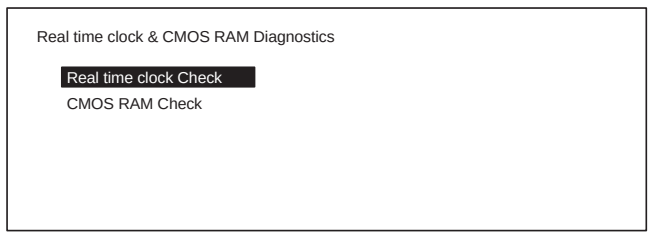
③ Terminating method

After the test result is displayed, press the Esc key to terminate and return to the ROM diagnostics menu.

3-5. Real time clock & CMOS RAM Diagnostics

RTC and CMOS RAM check is performed.

The following menu is displayed. The highlighted cursor is moved by the cursor keys (UP ↑ and DOWN ↓) of the AT keyboard. Move the cursor to the desired item, and the press the Enter key to execute the selected diagnostics program. When the selected diagnostics program is completed. Pressing Esc key again returns to the service diagnostics menu.



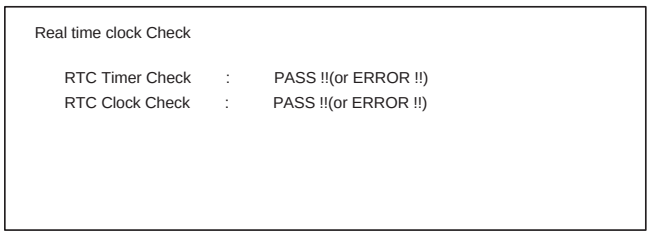
1) Real time clock Check

① Checking content

RTC timer function and RTC clock function are tested.

In RTC timer check, the RTC timer is set so that an interrupt is generated after 2 sec and check that the interrupt is performed properly. In RTC clock check, the RTC clock is set to 23:59:58, 31/Dec/1989, and checks that the clock shows 0:0:0, 1/Jan/1990 after 2 sec.

② Display



③ Terminating method

After the test result is displayed, press Esc key to terminate and return to the RTC and CMOS RAM diagnostics menu.

2) CMOS RAM Check

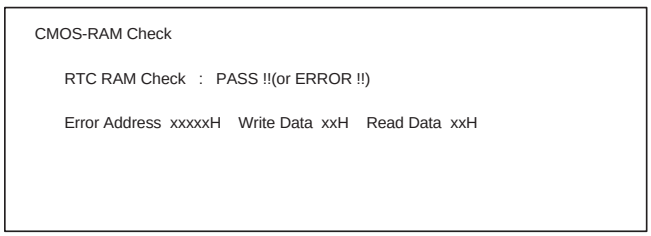
① Checking content

The read/write check is performed for CMOS-RAM when setting up. The checking procedure is as follows:

i. Test address data is saved to the main memory.
ii. Test data 55H is written to the test address.
iii. Test data and read data are compared, and test data AAH is written to the test address.
iv. Test data and read data are compared.
v. The saved test data is written to the test area.
vi. The address is incremented until it becomes 3FH.

If POFF interruption is generated during the test, the test is stopped and the saved data is written to the test area within 50ms.

② Display



The error address and the error bit are displayed only when an error occurs. (When no error occurs, they are not displayed.)

③ Terminating method

After the test result is displayed, press Esc key to terminate and return to the RTC and CMOS RAM diagnostics menu.

3-6. Touch Panel Diagnostics

The touch panel and its controller are checked. Communication with the controller is performed by 8250 built in the gate array PSC2.

The controller diag check, the touch keypad test, and the linearity test are performed.

The initial display is as follows:

1) Controller Diag Test

① Checking content

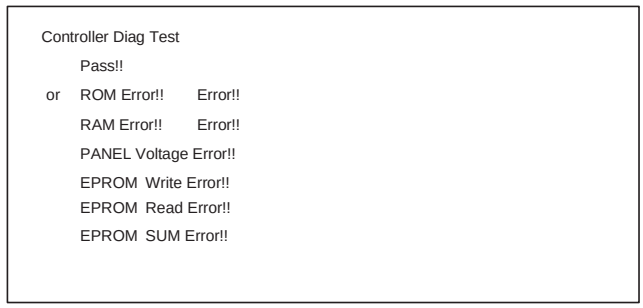
After initializing the controller, the diagnostic command is executed. The procedures are as follows:

- One byte of dummy data (FFh) is sent and a wait state of 100ms is made.
- The reset command (80h) is sent and a wait state for the end code (2 bytes: 90h and 00h) from the controller is made.
- The diagnostic command (2 bytes: 89h, any one-byte data) is executed, and a wait state for the end code (3 bytes: 90h, return code, any one-byte data) is made.
- If an error occurs the error display is made with the return code.

∗ To exit from the controller diagnostic test. press the Esc key during the wait state for the end code response.

Return code	Content
0Ah	ROM error
0Bh	RAM error
0Ch	Panel voltage error
0Dh	Reserve
0Eh	EPROM write error
0Fh	EPROM read error
10h	EPROM check sum error

② Display



③ Terminating method

After the test result is displayed, press the Esc key to terminate and return to the Touch panel diagnostics menu.

2) Touch Key Pad Test

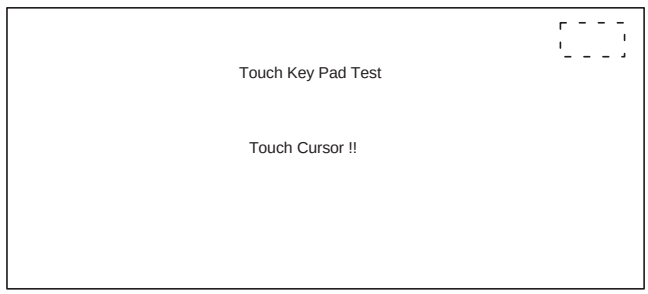
① Checking content

The driver function call is used.

[ ] is displayed at the four corners of the LCD sequentially.
(In the sequence of upper right, upper left, lower left, lower right.)

When the [ ] is touched by the operator, the buzzer sounds and the screen turns to ■ .

② Display



③ Terminating method

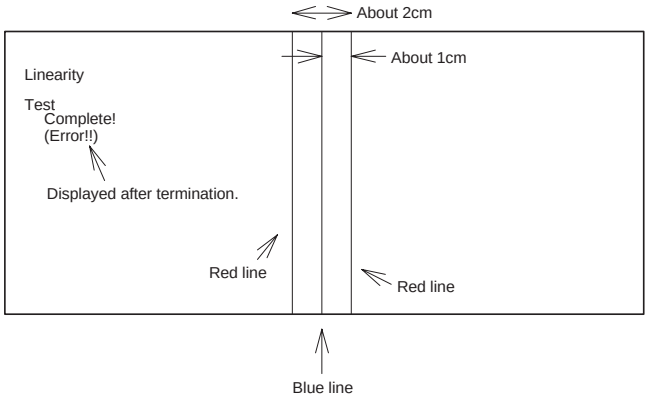
Touch all four [ ] or press the Esc key to terminate and return to the Touch panel diagnostics menu.

3) Linearity test

① Checking content

Red lines are displayed at both sides of the blue line at the center. The operator must touch the blue line without touching the red lines and drag from top to bottom.
The touched part of the blue line is changed to white.
If the red line is touched, an error message is issued.

② Display



③ Terminating method

Press Esc key to terminate and return to the Touch panel diagnostics menu.

3-7. Clerk Key Diagnostics (Not used for "U" version)

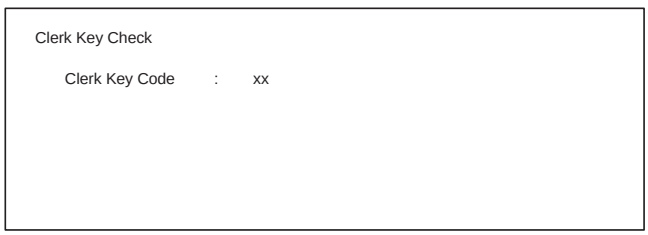
The clerk key input test is performed.
Pressing the Esc key returns to the serviceman diagnostics menu.

1) Clerk Key Check

① Checking content

Key code inserted to the clerk key switch which is then displayed in a decimal value.

② Display



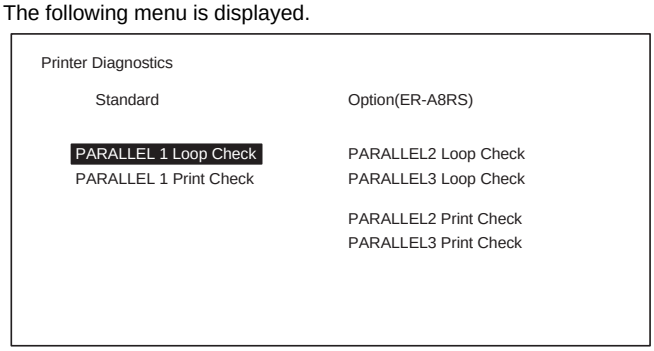
The clerk code is displayed at XX.

③ Terminating method.

Press the Esc key to terminate and return to the Serviceman's diagnostics menu.

3-8. Printer Diagnostics

The parallel interface (standard) and ER-A8RS parallel interface (option) are tested.
Here, the parallel interface on the main body is mentioned as PARALLEL1, and the parallel interface on ER-A8RS as PARALLEL 2/3.
The following menu is displayed.



The highlighted cursor is moved by the cursor keys (UP ↑ and DOWN ↓) of the AT keyboard. Move the cursor to the desired item, and press the Enter key to execute the selected diagnostics program.

When the selected diagnostics program is completed, the display returns to the menu screen. Pressing the Esc key returns to the serviceman diagnostics menu.

1) PARALLEL1 Loop Check

① Checking content

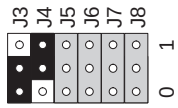
A loop check is made for the standard I/O address 378H ~ 37FH. (PARALLEL1)

In the loop check, a normally-operating ER-A8RS is inserted and the loop cable (UKOG-6717RCZZ) is connected between PARALLEL1 and PARALLEL3 (ER-A8RS) for testing. Set the jumpers on the PWB prior to the test as follows:

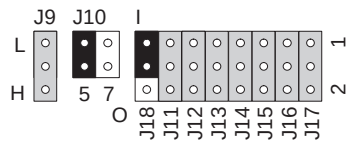
Signal name	Pin No.
STROBE-	1
DB0	2
DB1	3
DB2	4
DB3	5
DB4	6
DB5	7
DB6	8
DB7	9
ACK-	10
BUSY	11
PE	12
SLCT	13
AUTOFD-	14
ERROR-	15
INIT-	16
SLCTIN-	17
GND	18~2

Pin No.	Signal name
1	STROBE-
2	DB0
3	DB1
4	DB2
5	DB3
6	DB4
7	DB5
8	DB6
9	DB7
10	ACK-
11	BUSY
12	PE
13	SLCT
14	AUTOFD-
15	ERROR-
16	INIT-
17	SLCTIN-
18~2	GND

Loop cable (UKOG-6717RCZZ) wiring diagram



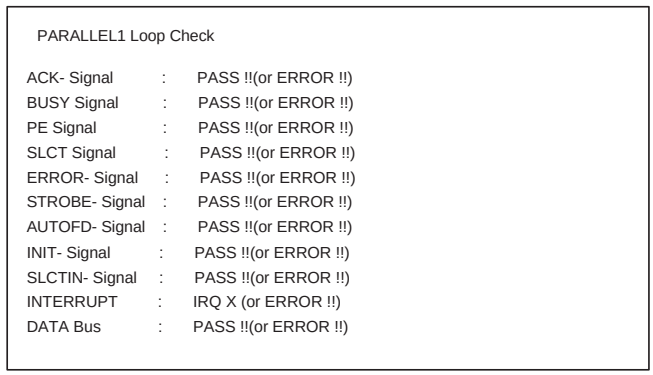
UP-5300 : PARALLEL1 OUTPUT MODE
A8RS : PARALLEL3 INPUT MODE



Opposite ER-A8RS setting

Jumper pin setting diagram

② Display


PARALLEL1 Loop Check
ACK- Signal : PASS !!(or ERROR !!)
BUSY Signal : PASS !!(or ERROR !!)
PE Signal : PASS !!(or ERROR !!)
SLCT Signal : PASS !!(or ERROR !!)
ERROR- Signal : PASS !!(or ERROR !!)
STROBE- Signal : PASS !!(or ERROR !!)
AUTOFD- Signal : PASS !!(or ERROR !!)
INIT- Signal : PASS !!(or ERROR !!)
SLCTIN- Signal : PASS !!(or ERROR !!)
INTERRUPT : IRQ X (or ERROR !!)
DATA Bus : PASS !!(or ERROR !!)

The interruption level is displayed at X.

When no access is allowed to PARALLEL1, the following display is made.

```
PARALLEL1 Loop Check

    PARALLEL1 Channel Disabled
```

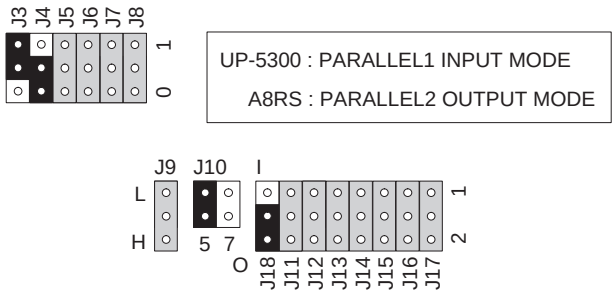
③ Terminating method.

Press the Esc key to terminate and return to the Printer diagnostics menu.

2) PARALLEL2 Loop Check

① Checking content

A loop check is performed for ER-A8RS I/O address 278H ~ 27FH (PARALLEL2), In the loop check, the loop cable shown in Fig, 3-4 is connected between PARALLEL2 (ER-A8RS) and PARALLEL1 for testing. Set the jumpers on the PWB prior to the test as shown in Fig. 3-6.



Setting of ER-A8RS to be tested

Fig. 3-6 Jumper pin setting

② Display

```
PARALLEL2 Loop Check

ACK- Signal      :    PASS !!(or ERROR !!)
BUSY Signal      :    PASS !!(or ERROR !!)
PE Signal        :    PASS !!(or ERROR !!)
SLCT Signal      :    PASS !!(or ERROR !!)
ERROR- Signal    :    PASS !!(or ERROR !!)
STROBE- Signal   :    PASS !!(or ERROR !!)
AUTOFD- Signal   :    PASS !!(or ERROR !!)
INIT- Signal     :    PASS !!(or ERROR !!)
SLCTIN- Signal   :    PASS !!(or ERROR !!)
INTERRUPT        :    IRQ X (or ERROR !!)
DATA Bus         :    PASS !!(or ERROR !!)
```

The interruption level is displayed at XX.

If no access is allowed to PARALLEL2, the following display is made.

```
PARALLEL2 Loop Check

    PARALLEL2  Channel Disabled
```

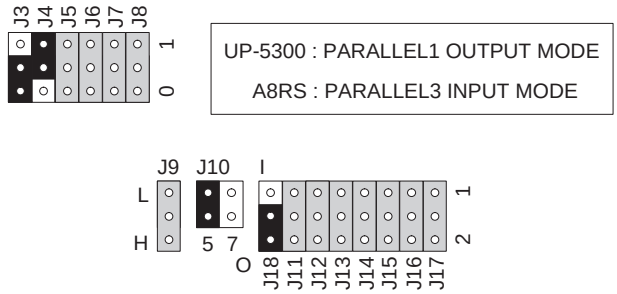
③ Terminating method.

Press the Esc key to terminate and return to the Printer diagnostics menu.

3) PARALLEL3 Loop Check

① Checking content

A loop check is performed for ER-A8RS I/O address 3BCH ~ 3BEH (PARALLEL3), In the loop check, the ER-A8RS to be connected is connected to the extension slot and the loop cable shown in Fig. 3-4 is connected between PARALLEL3 (ER-A8RS) and PARALLEL1 for testing. Set the jumpers on the PWB prior to the test as shown in Fig. 3-6.



Setting of ER-A8RS to be tested

Fig. 3-6 Jumper pin setting

② Display

```
PARALLEL3  Loop Check

ACK- Signal      :    PASS !!(or ERROR !!)
BUSY Signal      :    PASS !!(or ERROR !!)
PE Signal        :    PASS !!(or ERROR !!)
SLCT Signal      :    PASS !!(or ERROR !!)
ERROR- Signal    :    PASS !!(or ERROR !!)
STROBE- Signal   :    PASS !!(or ERROR !!)
AUTOFD- Signal   :    PASS !!(or ERROR !!)
INIT- Signal     :    PASS !!(or ERROR !!)
SLCTIN- Signal   :    PASS !!(or ERROR !!)
INTERRUPT        :    IRQ X (or ERROR !!)
DATA Bus         :    PASS !!(or ERROR !!)
```

The interruption level is displayed at XX.

If no access is allowed to PARALLEL3, the following display is made.

```
PARALLEL3 Loop Check

    PARALLEL3 Channel Disabled
```

③ Terminating method.

Press the Esc key to terminate and return to the Printer diagnostics menu.

4) PARALLEL1 Print Check

① Checking content

The print check is performed for the standard port PARALLEL1 at I/O address 378H ~ 37FH. In the print check, the D-Sub 25 pin connector is connected with a printer to allow a print pattern test.

The test procedures are as follows:

i. Data of 55H is written to I/O address 378H, and the same address is read. If the read data is not 55H, "PARALLEL1 Channel Disabled" is displayed and the following check is not performed.

ii. Characters of 20H ~ 7FH (ASCII code) are printed and the line is changed.

This procedure is repeated for 5 times.

② Display

"PARALLEL1 Channel Disabled" is displayed only when no access to PARALLEL1 is allowed.

③ Terminating method.

Press the Esc key to terminate and return to the Printer diagnostics menu.

5) PARALLEL2 Print Check

① Checking content

The print check is performed for PARALLEL2 at I/O address 278H ~ 27Fh on the ER-A8RS.

In the print check, set the short pin of the ER-A8RS to be tested as shown in Fig. 3-9, and connect the D-Sub 25 pin connector to a printer to allow a print pattern test.

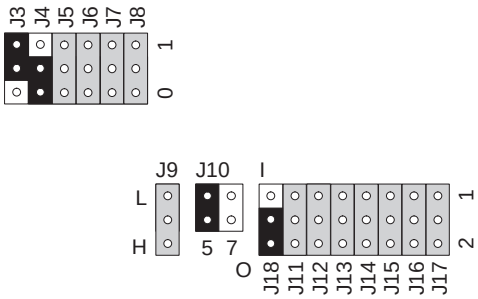


Fig. 3-9 Jumper pin setting

The test procedures are as follows:

i. Data of 55H is written to I/O address 278H, and the same address is read. If the read data is not 55H, "PARALLEL2 Channel Disabled" is displayed and the following check is not performed.

ii. Characters of 20H ~ 7FH (ASCII code) are printed and the line is changed.
This procedure is repeated for 5 times.

② Display

"PARALLEL2 Channel Disabled" is displayed only when no access to PARALLEL2 is allowed.

③ Terminating method.

Press the Esc key to terminate and return to the Printer diagnostics menu.

6) PARALLEL3 Print Check

① Checking content

The print check is performed for PARALLEL3 at I/O address 3BCH ~ 3BEh on the ER-A8RS.

In the print check, set the short pin of the ER-A8RS to be tested as shown in Fig. 3-10, and connect the D-Sub 25 pin connector to a printer to allow a print pattern test.

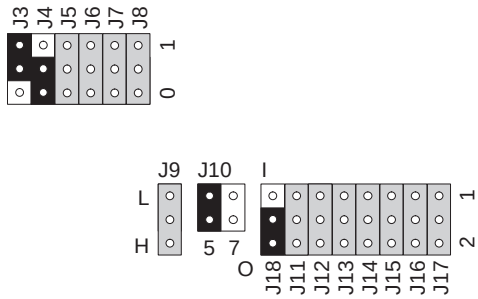


Fig. 3-10 Jumper pin setting

The test procedures are as follows:

i. Data of 55H is written to I/O address 3BCH, and the same address is read. If the read data is not 55H, "PARALLEL3 Channel Disabled" is displayed and the following check is not performed.

ii. Characters of 20H ~ 7FH (ASCII code) are printed and the line is changed.
This procedure is repeated for 5 times.

② Display

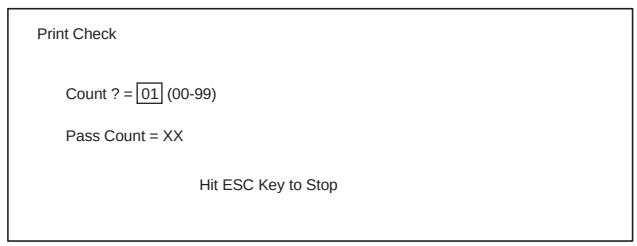
"PARALLEL3 Channel Disabled" is displayed only when no access to PARALLEL3 is allowed.

③ Terminating method.

Press the Esc key to terminate and return to the Printer diagnostics menu.

7) UP-T80BP Test

① Display



On the above screen the setting appears in the box.
The Count can be set from "01" up to "99". If "00" is set, printing does not stop until the ESC key is pressed.

② Testing

The following patterns are printed and the paper cut command is sent by the specified number of times to the Serial 5 of I/O address 980H to 987H..

③ Error message

The following error message appears if a communication error occurs with the UP-T80BP.

```
Print Check

********** UP-T80BP I/F ERROR **********

Hit ESC Key to Stop
```

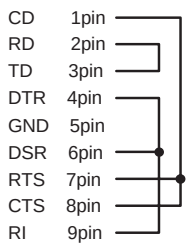
④ End of testing

The testing is finished after printing is made by the specified number of times or by pressing the ESC key.

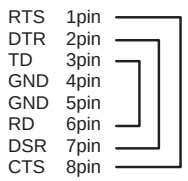
3-9. Serial I/O Diagnostics

The serial interface of UP-5300 and the option PWB ER-A8RS is performed. To test the 9pin D-Sub port, connect the D-Sub loop back connector (UKOG-6705RCZZ).

To test the RJ45 port, connect the loop back connector (UKOG-6729BHZZ).



Loop back connector (UKOG-6705RCZZ) wiring diagram



Loop back connector (UKOG-6729BHZZ) wiring diagram

The UP-5300's 9-pin D-sub ports are used as COM1 and 2. In addition, the UP-5300's RJ45 ports are used as COM3 and 4 or COM5 and 6 according to the setup. On the other hand, ER-A8RS is used by selecting either COM1 and 2 or COM3 and 4 according to the setup.

Therefore, when an ER-A8RS is used, you must set COM1, 2, 5, and 6 on the UP-5300 side, and set COM3 and 4 on the ER-A8RS side.

The following menu is displayed.

The highlighted cursor is moved by the cursor keys (UP ↑ and DOWN ↓) of the AT keyboard. Move the cursor to the desired item, and press the Enter key to execute the selected diagnostics program.

When the selected diagnostics program is completed, the display returns to the menu screen. Pressing the Esc key returns to the serviceman diagnostics menu.

```
Serial I/O Diagnostics

  COM1 Check
  COM2 Check
  COM3 Check
  COM4 Check
  COM5 Check
  COM6 Check
```

1) COM1 Check

① Content

The loop back check is performed for the UART at I/O address 3F8H ~ 3FFH. The test procedures are as follows:

i. UART setting is made. If access is denied to UART at that time, "COM1 Disabled" is displayed and the following check is not performed.

ii. RTS signal is turned on/off to check that CD, CTS signal is normally operating. In case of any abnormality, ERROR is displayed.

iii. DTR signal is turned on/off to check that DSR, RI signal is normally operating. In case of any error, ERROR is displayed. When an error occurs in procedure i or ii, the following test is not performed.

iv. Set the baud rate to 19200bps asynchronous. 256 byte data of 00H ~ FFH is transmitted from SD signal. Data received at RD signal is compared to check that the both are the same. If the outputted data is not returned for 5 sec or more, ERROR is displayed and the test is terminated.

v. An interruption signal is issued from UART and the number of generated interruption request signal is displayed.

② Display

```
Serial I/O COM1 Check

RTS - CD     :   PASS !!(or ERROR !!)
RTS - CTS    :   PASS !!(or ERROR !!)
DTR - DSR    :   PASS !!(or ERROR !!)
DTR - RI     :   PASS !!(or ERROR !!)
TD - RD      :   PASS !!(or ERROR !!)
INTERRUPT    :   IRQ XX
```

The number of the interruption request signal is displayed at XX.

If no access is allowed to COM1 UART, the following display is made.

```
Serial I/O COM1 Check

  COM1 Channel Disabled
```

③ Terminating method.

Press the Esc key to terminate and return to the Serial I/O diagnostics menu.

2) COM2 Check

① Checking content

The loop back check is performed for the UART at I/O address 2F8H ~ 2FFH. The check procedure, the display, and the terminating method are the same as COM1 Check.

3) COM3 Check

① Checking content

The loop back check is performed for the UART at I/O address 3E8H. When the ER-A8RS is assigned to COM3, the check procedure, display and terminating method are the same as COM1.
When the RJ-45 port of the UP-5300 main unit is assigned to COM3, the following points are different from COM1 Check :

① Content
- RTS-CTS is not checked.
- DTR-RI is not checked.

② Display
- RTS-CTS is not displayed.
- DTR-RI is not displayed.

COM3 is checked as well as COM1 except the above 2 points.

4) COM4 Check

① Checking content

The loop back check is performed for the UART at I/O address 2E8H ~ 2EFH. The check procedure, the display, and the terminating method are the same as COM3 Check.

5) COM5 Check

① Checking content

The loop back check is performed for the UART at I/O address (PSC2 base address) + (410H ~ 417H). The following points are different from the COM1 Check:

① Content
- RTS-CTS is not checked.
- DTR-RI is not checked.

② Display
- RTS-CTS is not displayed.
- DTR-RI is not displayed.

COM5 is checked as well as COM1 except the above 2 points.

6) COM6 Check

① Checking content

The loop back check is performed for the UART at I/O address (PSC2 base address) + (418H ~ 41FH). The checking procedure, the display, and the terminating method are the same as COM5 Check.

3-10. Liquid Crystal Display Diagnostics

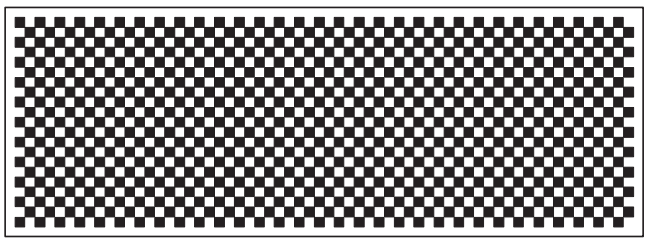
LCD test is performed.
The following patterns are displayed in sequence. Pressing the space bar proceeds to the next display. Pressing the space bar at the final pattern or pressing the Esc key during the test, will return the display to the service diagnostics menu.

1) Liquid Crystal Display Check

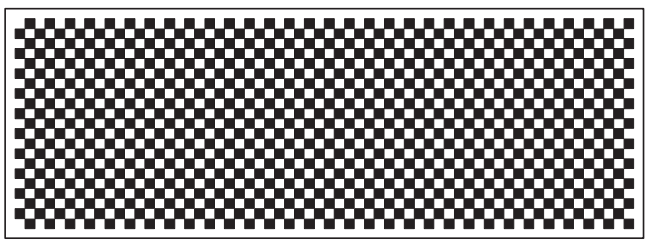
① Checking content

The test patterns are displayed in the following test procedures. Pressing the space bar moves to the next pattern.

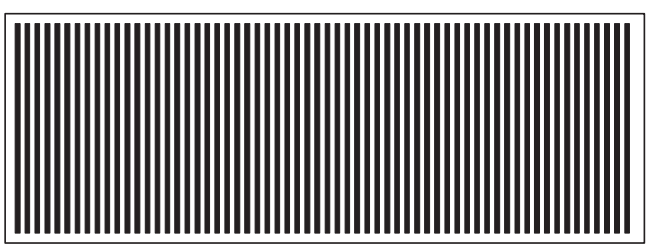
i. Black-and-white pattern in 1 dot interval



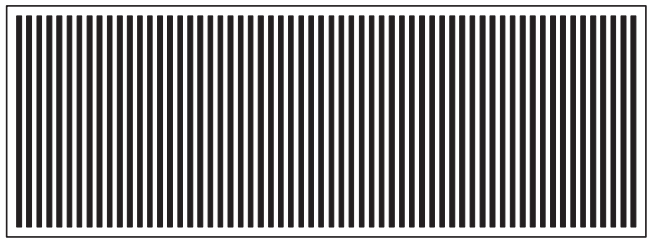
ii. Reversed pattern of pattern i.



iii. Vertical stripe pattern in 1 dot interval

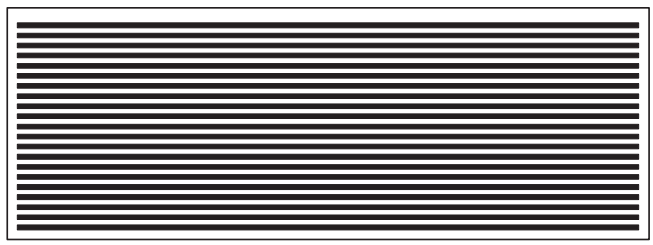


iv. Reversed pattern of pattern iii.

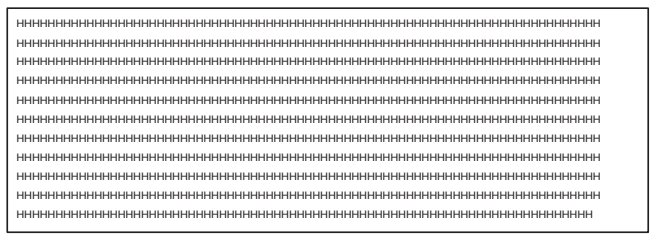


v. Horizontal stripe pattern in 1 dot interval

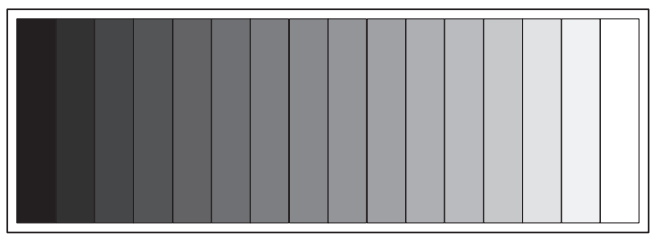
vi. Reversed pattern of pattern v.



vii. "H" pattern (80 digits × 35 lines) In the 35th line, only 78 digits of "H" are displayed.
(The actual display range is 25 lines. Scroll for 10 lines to check.)

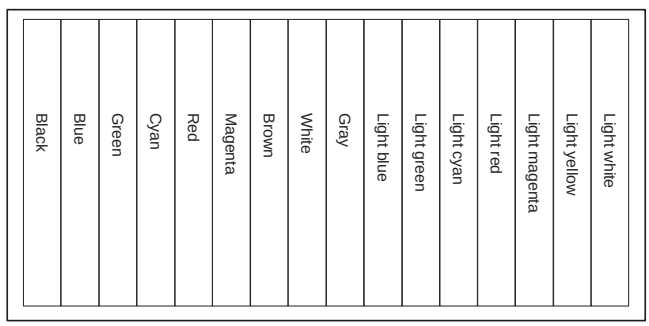


viii. Gradation pattern from black to white in 16 gradations



ix. All white pattern

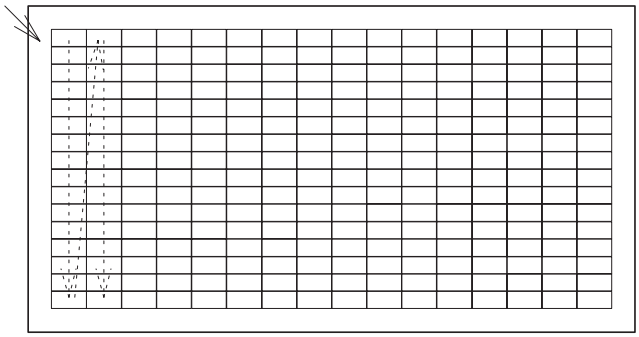
x. Color bar (16 colors)
Color bars of 16 colors are displayed.



xi. Color pattern (256 colors)

Color pattern of 256 colors is displayed. The displayed colors are the default pallet.

Arrange RAMDAC register No. 0 ~ 255 from the upper left.



xii. Backlight OFF

The backlight is turned off without turning off the display.

xiii. Backlight ON

② Terminating method

Press the space bar or Esc key to terminate and return to the Serviceman's diagnostics menu.

3-13. Magnetic Card Reader Diagnostics

This test program reads the magnetic card based on the ISO7811/1-5 standard and displays the data.

Pressing the Esc key returns to the service diagnostics menu.

1) Magnetic Card Reader Check

① Checking content

The test program reads tracks 1 and 2 of the magnetic card (UKOG-6718RCZZ) based on the ISO7811/1 ~ 5 standard, and displays the data in ASCII code. There are two kinds of data patterns to be read.

TRACK 1: IATA pattern
76 character 7bit/character (Max. 79 character)

TRACK 2: ABA data pattern
28 character, 5bit/character (Max. 40 character)

To read the card data, the following setting is performed.

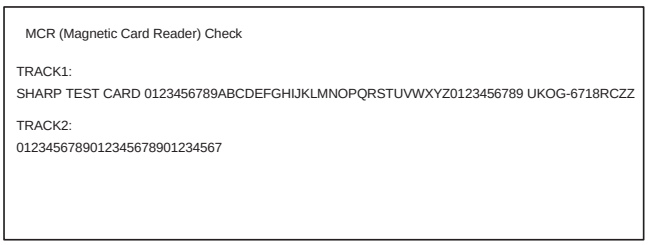
- Mode set
  46h is set to PSC2 channel 1 mode set register. (IATA, 6bit)
  74h is set to PSC2 channel 2 mode set register. (ABA, 4bit)
- Start mark set
  45h is set to PSC2 channel 1 start mark register.
  0Bh is set to PSC2 channel 2 start mark register.
- Interrupt reset
  Dummy data is written to PSC2 channel 2 start mark register.
- Interrupt mask cancel 01h is written to PSC2 MCR mask register to cancel mask.

  In addition, setting for the PSC2 extension interruption is performed.

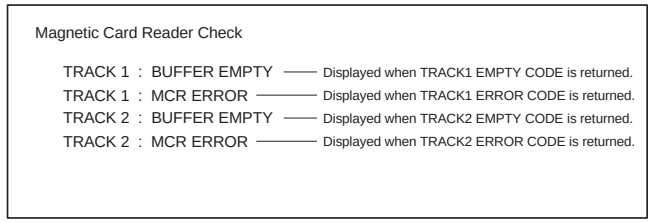
  When the card is scanned, the obtained data is written to the FIFO buffer from the start mark to LRC in sequence. Then, the card data is read by interrupt process.

  After reading data, the FIFO buffer is reset.

② Display



The above display is made when the card (UKOG6718RCZZ) is passed through the MCR. In case of an error, the error code is displayed as follows:


Magnetic Card Reader Check
TRACK 1 : BUFFER EMPTY —— Displayed when TRACK1 EMPTY CODE is returned.
TRACK 1 : MCR ERROR —— Displayed when TRACK1 ERROR CODE is returned.
TRACK 2 : BUFFER EMPTY —— Displayed when TRACK2 EMPTY CODE is returned.
TRACK 2 : MCR ERROR —— Displayed when TRACK2 ERROR CODE is returned.

③ Terminating method

Press the Esc key to terminate the test and return to the Serviceman's diagnostics menu.

3-14. System Switch Diagnostics

The system switch information of the main PWB is displayed.

Pressing the Esc key returns to the serviceman diagnostics menu.

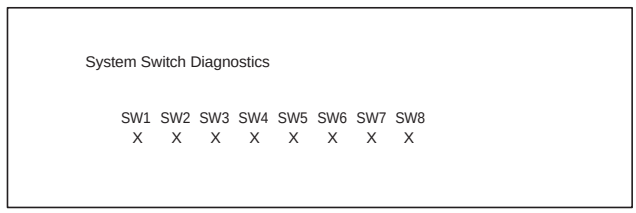
1) System Switch

① Checking content

The system switch reads I/O address 7F0H every 10ms to display the value of bit 0 ~ 7. The relationship between the bit and SW is as shown in the table below.

Bit	7	6	5	4	3	2	1	0
7F0H	SW8	SW7	SW1	SW2	SW3	SW4	SW5	SW6

② Display



Each SW data is displayed at X. If bit data is "1," the display is "OFF". If bit data is "0," the display is "ON".

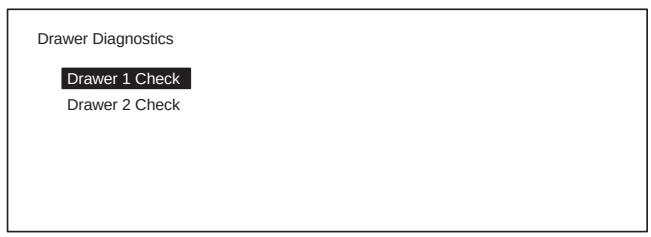
③ Terminating method

Press the Esc key to terminate the test and return to the Serviceman's diagnstics menu.

3-15. Drawer Diagnostics

The drawer open and sensor test are executed.

The following menu is displayed. The highlighted cursor is moved by the cursor keys (UP ↑ and DOWN ↓) of the AT keyboard. Move the cursor to the desired item, and press the Enter key to execute the selected diagnostics program. When the selected diagnostics program is completed, the display returns to the menu screen. Pressing the Esc key returns to the service diagnostics menu.



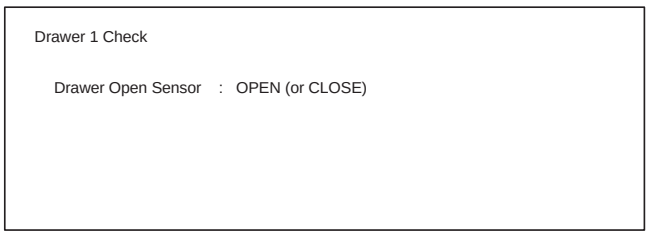
1) Drawer 1 check

① Checking content

The drawer 1 solenoid is turned on and the drawer open sensor value is sensed at every 100ms and the state is displayed.

When Drawer 1 and Drawer 2 are connected, "CLOSE" is displayed only when both the drawers are closed.

② Display



③ Terminating method

Press the Esc key to terminate the test and return to the Drawer diagnostics menu.
Pressing the ESC again will return to the serviceman's diagnostics menu.

2) Drawer 2 Check

① Checking content

Drawer 2 solenoid is turned on and the drawer open sensor value is sensed at every 100ms and the state is displayed.
When Drawer 1 and Drawer 2 are connected, "CLOSE" is displayed only when both the drawers are closed.

② Display

Same as Drawer 1.

③ Terminating method

Same as Drawer 1.

3-16. Option Display Diagnostics

The option display includes a microprocessor inside that allows communication with the host by RS232 conforming interface.
PSC2 UART4 is used on the main body side.
Communication conditions are as follows:

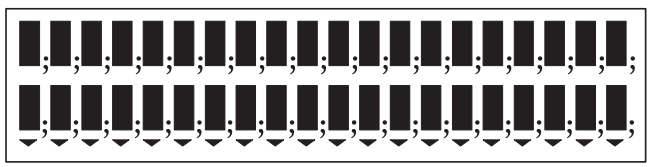
- Data length: 8 bit
- Parity (Yes/No): No
- Baud rate: 9600bps

① Checking content

The test patterns are displayed in the sequence shown below. Pressing the space bar moves to the next pattern.

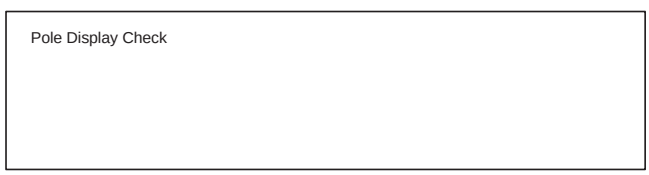
i. The following test patterns are displayed.

ii. The test pattern with all digits ON is displayed.



iii. All OFF

② Display



③ Terminating method

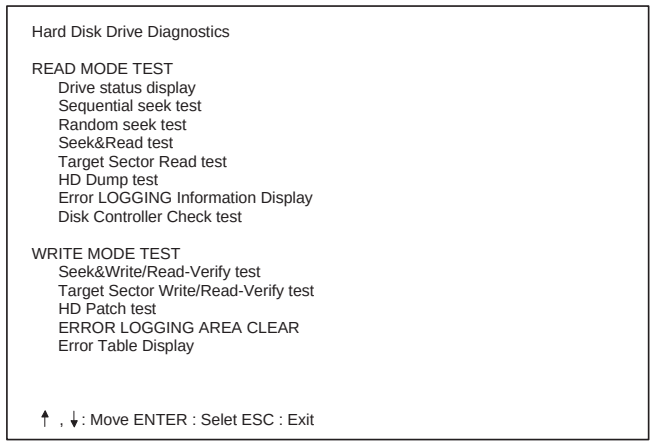
Press the Esc key to turn off FD display and terminate the test and return to the Option display diagnostics menu and the test is terminated.

3-17. IDE I/F & Hard Disk Diagnostics

The hard disk is tested and the information stored in the hard disk is displayed.
The following tests are executed.

- Read test: Seek (sequential, random) test, read only (target cylinder, target sector), and dump test
- Write test: Write verify test (target cylinder, target sector), and batch test.
- Other functions: Drive status display, controller check, error logging area (error information) display, and error information display

Test screen (service repair only)



On the above screen, select the desired test item with ↑ (UP) and ↓ (DOWN) keys and press the Enter key to execute the test. Pressing the Esc key returns to the initial menu.

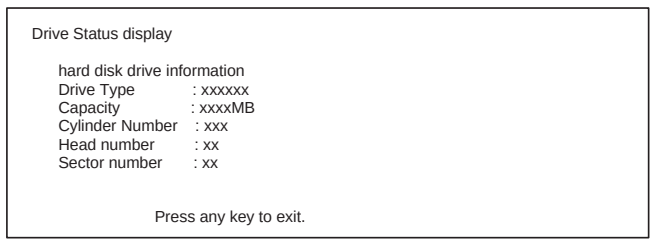
[READ MODE TEST]

1) Drive Status display

① Checking content

The hard disk drive standard values (Memory capacity, Number of cylinders. Number of heads, and Number of sectors) are displayed.

② Display



Drive type:	Hard disk drive name
Capacity:	Hard disk memory capacity
Cylinder number:	Max. cylinder number
Head number:	Max. head number
Sector number:	Max. sector number

③ Terminating method

Press any key to terminate the test and return to the menu screen in the previous (1).

2) Sequential Seek Test

[Test conditions setting]

- Cylinder Range [0 ~ inmost cylinder]

  The cylinder range to be tested is set.
- Retry Count [0 ~ 4]

  Retry count in case of an error is set.
- Error Stop/Continue/1 Pass

  Selection is made among Error Stop/Continue/1 Pass in case of an error.

- Test Start ? [Yes/No]

  Selection is made to execute the test or not.

① Checking content

In the cylinder range set above, the sequential seek is executed for every 1 track. When the seek test in the set range is completed (in the direction of 0 → inmost cylinder), it is counted as 1 pass. In case of an error during the above test, a retry is repeated up to the set number of retries. Every time an error occurs by executing retry up to the retry number and error logging is performed. Logging is made for HD and DRAM.

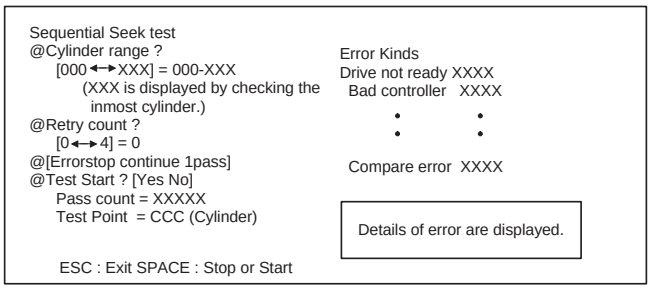
When an "Error stop" is set in the test conditions setting, and an error occurs during the above test, the error display is made and the test is stopped. Press the space bar to resume the test.

When "Continue" is set, even if an error occurs, the error display is made but the test is not stopped.

When "1 Pass" is set, a series of tests is made only once and the test is stopped.

② Display

Sequential Seek test execution screen


Sequential Seek test
@Cylinder range ?
[000 ◄►XXX] = 000-XXX
(XXX is displayed by checking the inmost cylinder.)
@Retry count ?
[0 ◄►4] = 0
@[Errorstop continue 1pass]
@Test Start ? [Yes No]
Pass count = XXXXX
Test Point = CCC (Cylinder)
ESC : Exit SPACE : Stop or Start
Error Kinds
Drive not ready XXXX
Bad controller XXXX
Compare error XXXX
Details of error are displayed.

Select the desired items at the position of @. (@ is not displayed on the screen.)

On the above screen, when the pass count is counted up (when the point is counted up to the upper limit set in the cylinder range setting, the pass count is counted up by 1.), and if the error counter of all error items are not counted up (remaining as 00000), the test is OK.

When the space bar is pressed during the test, the test is interrupted.

When the space bar is pressed during interruption of the test, the test is started.

③ Terminating method

Press the Esc key during execution of the test or during interruption of the test to terminate the test and return to the above menu screen.

3) Random Seek Test

[Test condition setting]

Same as the above sequential read.
However, execution of the test by 1 Pass means execution of random seek through the set cylinder range.

① Checking content

The random seek is executed for every one track in the cylinder range set previously.

When the seek test is completed in the set range, it is counted as 1 pass.

In case of an error during the above test, a retry is repeated up to the set number of retries. Every time an error occurs a retry is performed up to the set number of retries and, error logging is made. Logging is made for HD and DRAM.

When the "Error Stop" is set in the test condition setting, and an error occurs during the above test, the error display is shown and the test is interrupted. Press the space key to resume the test.

When the "Continue" is set, even if an error occurs, the error display is made but the test is not stopped.

When "1 Pass" is set, a series of tests is made only once and the test is stopped.

② Display

Same as the above sequential read, however the following contents are different.

The test Point is changed at random in the range of 000 ~ XXX (cylinder range set value).

Each point is tested once, and the pass count is added by one with XXX times.

③ Terminating method

Press the Esc key during execution of the test or during interruption of the test to terminate the test and return to the above menu screen.

4) Seek & Read Test

[Test condition setting]

Same as the above sequential read. The following setting is additionally required.

- Sector count [0 ~ final sector]

The sector range to be tested is set.

① Checking content

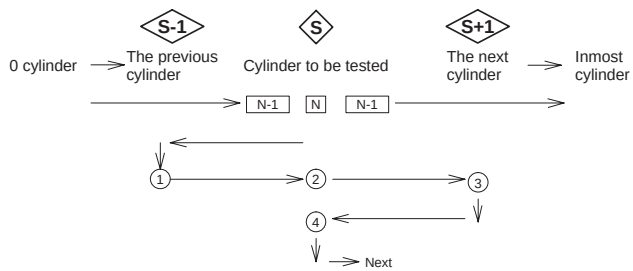
The sequential read for every one track is executed in the cylinder range and the sector range set above. (in the direction of 0 → inmost cylinder)

When the read test is completed in the set range, it is counted as 1 pass.

Before seeking, however, seek is made the previous cylinder and the following cylinder.

(Head movement)

When track N is read, the head moves as follows:



At ② and ④, read is executed.

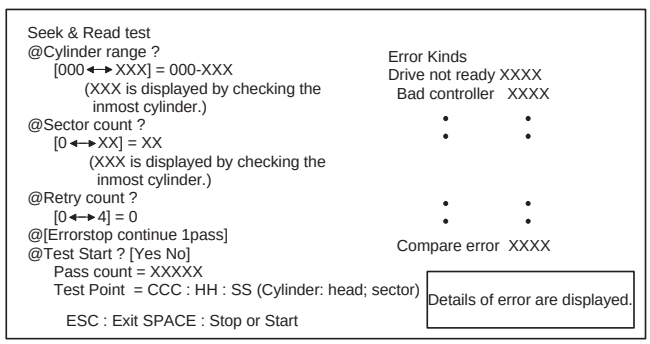
In case of an error during the above test, a retry is repeated up to the set number of retries. Every time an error occurs a retry is performed up to the set number of retries and, error logging is made. Logging is made for HD and DRAM.

When the "Error Stop" is set in the test condition setting, and an error occurs during the above test, the error display is shown and the test is interrupted. Press the space key to resume the test.

When the "Continue" is set, even if an error occurs, the error display is made but the test is not stopped.

When "1 Pass" is set, a series of tests is made only once and the test is stopped.

② Display


Seek & Read test
@Cylinder range ?
[000 ◄►XXX] = 000-XXX
(XXX is displayed by checking the inmost cylinder.)
@Sector count ?
[0 ◄►XX] = XX
(XXX is displayed by checking the inmost cylinder.)
@Retry count ?
[0 ◄►4] = 0
@[Errorstop continue 1pass]
@Test Start ? [Yes No]
Pass count = XXXXX
Test Point = CCC : HH : SS (Cylinder: head; sector)
ESC : Exit SPACE : Stop or Start
Error Kinds
Drive not ready XXXX
Bad controller XXXX
Compare error XXXX
Details of error are displayed.

Select the desired items at the position of @. (@ is not displayed on the screen.)

(On the above screen, the thick figures are selected, and the thick figure values are selected.)
On the above screen, when the pass count is counted up (when point is counted up to the upper limit set in the cylinder range setting, the pass count is counted up by 1.), and if the error counter of all error items are not counted up (remaining as 00000), the test is OK.

③ Terminating method

The methods to interrupt, resume, and terminate the test are the same as (2) Sequential read.

5) Target Sector Read Test

[Test conditions setting]

- Cylinder range [0 ~ inmost cylinder]

  The cylinder range to be tested is set.
- Head count [0 ~ final head]

  The head umber to be tested is set.
- Sector count [0 ~ final sector]

  The sector number to be tested is set.
- Retry count [0 ~ 4]

  Retry number incase of an error is set.
  - Error stop/Continue/1 Pass

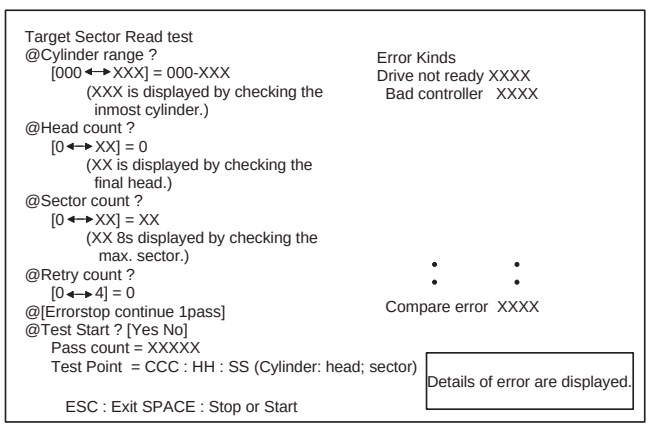
    Selection is made among Error Stop/Continue/1 Pass in case of an error.
  - Test start ? [Yes/No]

    Selection is made between Yes/No of test start.

① Checking content

A read is made for the cylinder range, the head number, and the sector number areas set in the above.
When the read test is completed in the set range, it is counted as 1 pass.
In case of an error during the above test, a retry is repeated up to the set number of retries. Every time when an error occurs a retry is performed up to the set number of retries and, error logging is made. Logging is made for HD and DRAM.
When the "Error Stop" is set in the test condition setting, and an error occurs during the above test, the error display is shown and the test is interrupted. Press the space key to resume the test.
When the "Continue" is set, even if an error occurs, the error display is made but the test is not stopped.
When "1 Pass" is set, a series of tests is made only once and the test is stopped.

② Display


Target Sector Read test
@Cylinder range ?
[000 ◄►XXX] = 000-XXX
(XXX is displayed by checking the inmost cylinder.)
@Head count ?
[0 ◄►XX] = 0
(XX is displayed by checking the final head.)
@Sector count ?
[0 ◄►XX] = XX
(XX 8s displayed by checking the max. sector.)
@Retry count ?
[0 ◄►4] = 0
@[Errorstop continue 1pass]
@Test Start ? [Yes No]
Pass count = XXXXX
Test Point = CCC : HH : SS (Cylinder: head; sector)
ESC : Exit SPACE : Stop or Start
Error Kinds
Drive not ready XXXX
Bad controller XXXX
Compare error XXXX
Details of error are displayed.

Select the desired items at the position of @. (@ is not displayed on the screen.)
(On the above screen, the thick figures are selected, and the thick figure values are selected.)
On the above screen, when the pass count is counted up (when point is counted up to the upper limit set in the cylinder range setting, the pass count is counted up by 1.), and if the error counter of all error items are not counted up (remaining as 00000), the test is OK.

③ Terminating method

The methods to interrupt, resume, and terminate the test are same as (2) Sequential read.

6) HD Dump Test

[Test conditions setting]

- Cylinder No. [0 ~ inmost cylinder]

  A certain cylinder No. to be displayed is set.
- Head No. [0 ~ final head]

  A certain head No. to be displayed is set.
- Sector No. [1 ~ final sector]

  A certain sector No. to be displayed is set.

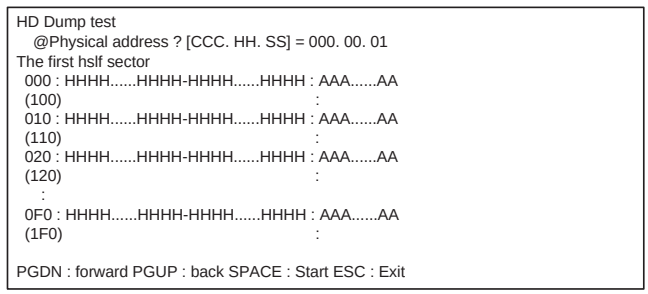
① Checking content

The sector set in the above is displayed on the screen in the unit of 256byte.

Hex data and ASCII characters are displayed.

By key operation, the following 256 byte data or previous 256byte data can be displayed.

② Display


HD Dump test
@Physical address ? [CCC. HH. SS] = 000. 00. 01
The first hslf sector
000 : HHHH.....HHHH-HHHH.....HHHH : AAA.....AA
(100) :
010 : HHHH.....HHHH-HHHH.....HHHH : AAA.....AA
(110) :
020 : HHHH.....HHHH-HHHH.....HHHH : AAA.....AA
(120) :
:
0F0 : HHHH.....HHHH-HHHH.....HHHH : AAA.....AA
(1F0) :
PGDN : forward PGUP : back SPACE : Start ESC : Exit

The physical address is set at the position of @. (On the above screen, the thick value is set.)

On the above screen, the first-half 256 byte at 000 cylinder, 00 head, and 01 sector is displayed.

Press the page down key to display the second-half 256 byte. (When the page down key is pressed on the above screen, the second-half 256byte at 000 cylinder, 00 head, and 01 sector is displayed.)

Press the page up key to display the first-half 256byte.

③ Terminating method

Press the Esc key to return to the menu screen of previous (1).

7) Error Information Display

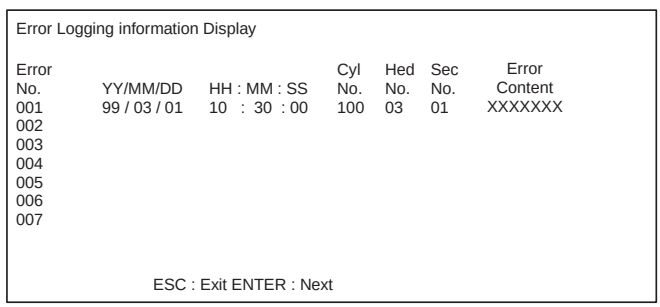
① Checking content

Error information stored in the inmost area of the HDD is displayed.

When the hard disk test is executed, error information stored in the error information storing area is displayed.

The inmost cylinder, 0 head, and 1 sector ~ 6 sector are read to be displayed.

② Display


Error Logging information Display
Error No. YY/MM/DD HH : MM : SS Cyl No. Hed No. Sec No. Error Content
001 99 / 03 / 01 10 : 30 : 00 100 03 01 XXXXXXX
002
003
004
005
006
007
ESC : Exit ENTER : Next

Every time the Enter key is pressed, the next page error information is displayed.

[Descriptions on the above screen]

Error No. ———— Error information register No. (001 ~)
(This is not an error code.)
YY/MM/DD———— Year/Month/Day
HH:MM:SS ——— Hour/Minute/Second
Cylinder ————— Cylinder No.
Head No. ———— Head No.
Sec No. ————— Sector No.
Error Content —— Error code is converted into error content and displayed.

③ Terminating method

Press the Esc key to return to the menu screen.

8) Controller check test

① Checking content

The diagnostic command included in the F-ROM is executed to perform hard disk controller check.

② Display

```
Disk Dontroller Check test
 @[Errorstop Continue 1pass]
 @Test Start ? [Yes No]

      Pass count = XXXXX

      Controller ..... Checking

ESC : Exit SPACE : Stop or Start
```

If the section [ ] blinks and the pass count is counted up, the test is OK.

When the space bar is pressed during the test, the test is interrupted.

When the space key is pressed during interruption of the test, the test is resumed.

③ Terminating method

When the Esc key is pressed during the test or test interruption, the test is terminated and the display returns to the menu screen.

[Write mode test]

(Note) When the following test is executed, the HDD data is destroyed.

The display shown before executing write mode test

```
When executed, Data on hard disk will be destroyed.
      Password ?  [*****]        ↑ Note message

ESC : Exit
```

Before executing the write mode test, "When executed, Data on hard disk will be destroyed." is displayed.

Password entry is urged. Only when the correct password is entered, does the display go to the next one.

The correct password is "sharp" or "SHARP" in 5 digits. When typing the correct password, the content is not displayed but "∗" is displayed.

9) Seek & Write/Read-Verify Test

[Test conditions setting]

Similar to the above 4). Cylinder range setting is 000 ↔ inmost cylinder 2.

① Checking content

For all the cylinder range and the sector range set in the above, the worst pattern data is written sequentially for every one track.

Then, the read/verify check is made for every one track.

The number of the read/verify check is one.

(Test for 1 pass)

The write is made in the direction of 0 → inmost cylinder.

The read/verify check is made in the direction of 0 → inmost cylinder.

The write is made in the direction of inmost cylinder → 0.

The read/verify check is made in the direction of inmost cylinder → 0.

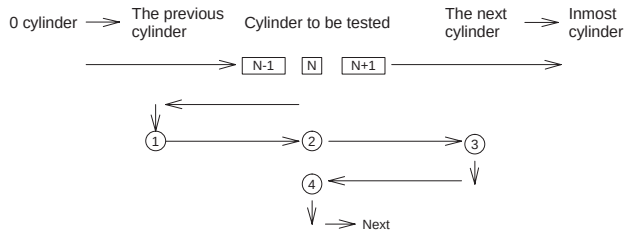
When writing data, write different data from the original stored data.

Before writing or reading, the head is moved to the previous or the following cylinder.

(Head movement)

When track N is read, the head moves as follows. (The head arm is deflected back and forth.)

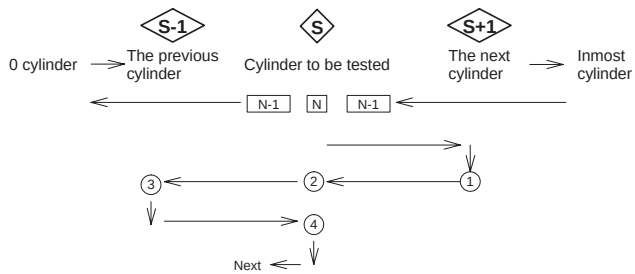
In the direction of 0 → inmost cylinder



Writing is made at ②.

Reading is made at ② and ④.

In the direction of 0 ← inmost cylinder



Writing is made at ②.

Reading is made at ②. and ④.

(Worst pattern data)

There are two kinds of worst data: B6DBH and 6DB6.

In case of an error during the above test, a retry is repeated up to the set number of retries. Every time an error occurs a retry is performed up to the set number of retries and, error logging is made. Logging is made for HD and DRAM.

When the "Error Stop" is set in the test condition setting, if an error occurs during the above test, the error display is shown and the test is interrupted. Press the space key to resume the test.

When the "Continue" is set, even if an error occurs, the error display is made but the test is not stopped.

When "1 Pass" is set, a series of tests is made only once.

② Display

Same as the previous (4). The following two points are different.

∗ Cylinder range ?

[000 ↔ XXX] (XXX is inmost cylinder 2.)

∗ Test mode: [ ] is displayed.

When data writing, WRITE is displayed in [ ]. When data reading, READ is displayed.

③ Terminating method

Same as (4).

10) Target Sector Write/Read-verify Test

[Test conditions setting]

Similar to the previous 5). Cylinder range setting is 000 ↔ (Final cylinder 2).

① Checking content

For the cylinder range, the head number, and the sector number area set in the above, write/read/verify is made.

When the write/read test is completed in the set range, it is counted as 1 pass.

In case of an error during the above test, a retry is repeated up to the set number of retries. Every time an error occurs a retry is performed up to the set number of retries and, error logging is made. Logging is made for HD and DRAM.

When the "Error Stop" is set in the test condition setting, if an error occurs during the above test, the error display is shown and the test is interrupted. Press the space key to resume the test.

When the "Continue" is set, even if an error occurs, the error display is made but the test is not stopped.

When "1 Pass" is set, a series of tests is made only once.

② Display

Same as the previous (6). The following two points are different.

∗ Cylinder range ?

[000 ↔ XXX] (XXX is inmost cylinder 2.)

∗ Test mode: [ ] is displayed.

When data writing, WRITE is displayed in [ ] . When data reading, READ is displayed.

③ Terminating method

Same as 5).

11) HD Patch Test (Utility)

[Test conditions setting]

Similar to the previous 6). The cylinder range setting is 000 ↔ (Final cylinder 2).

① Checking content

The sector set in the above is displayed on the screen in the unit of 256byte.

Hex data and ASCII characters are displayed.

By key operation, the following 256 byte data or previous 256byte data can be displayed.

After changing data on the screen, data is written to the selected set position.

② Display

Similar to the previous 6). Data in the HDD can be patched.

Patching is made as follows:

To patch data in the HD, change data on the screen.

(Move the cursor with ↑, ↓, ←, →, keys and enter data with 0 ~ F key.

Then select "Yes" in "Up data ? [Yes/No]" and press Enter key. (Move with ← key.)

With the above procedure, patch is made.

③ Terminating method

Same as 6).

12) Error Logging Area Clear

① Checking content

The last cylinder area in the HD is cleared with 00H.
(Error logging area: last cylinder, all sectors of 0 head)
The areas to be cleared with 00H is the last cylinder and all the sectors of 0 head.

② Display

```
Error Logging Area Clear

@Test Start ? [Yes No]  ◄— At first No is highlighted.


←, →: Move ESC : Exit ENTER : Select  ◄— Guidance before execution of the test
ESC : Exit SPACE : Retry              ◄— Guidance after execution of the test
```

Select "Yes" at position @ (move with ← key) and press the Enter key to execute the test.

When the test is executed once, the mode enters the key waiting mode. After executing the test, press the space key to execute again.

③ Terminating method

Press the Esc key to return to the menu screen.

13) Error table display

When an error occurs during the above test, error information is stored in the DRAM and the content is displayed.

If there is no error, OK or NO ERROR is displayed.

14) Supplemental items

Error information is stored up to 44 items in the sequence of occurrence from when the function is selected. If the item number exceeds 44, the error information is not stored any more.

15) Error content

The following error content is error information directly obtained from the HDD controller.

[Error code and meaning]

Error code	Error message
0	OK (This message is displayed when the test is normally completed.)
1	Drive not ready (HDD is not ready. STATUS REG bit 6 : 0)
2	Bad controller (HDD controller abnormality, diag status error STATUS REG bits : 1 or DIAG STATUS >= 2)
3	Track 000 Error (TRACK 000 cannot be found with RESTORE command. ERROR REG bit 1 : 1)
4	Seek Error (A seek error occurs. After STATUS COMMAND is executed, STATUS REG bit 4 : 0)
5	ID not Found (ID field is not detected. ERROR REG bit 4 : 0)
6	Data Address Mark not Found (Data Address Mark is not found. ERROR REG bit 0 : 1)
7	Bad Block Detect (BAD block mark is stored in the ID field of request sector. ERROR REG bit 7 : 1)
8	Uncorrectable error (An uncorrectable read error occurs. ERROR REG bit 6 : 1)
9	Others error (The other error STATUS REG bit 0 : 1, and ERROR REG : 0)
10	Time out error (Time out occurs when making access to HDD.)
11	Compare error (The written data and the read data are not the same.)

16) Error information storing area

① Error information storing area for diagnostics

1 sector ~ 6 sector of 0 head of the last cylinder is used.

Used in the following format from the head of each sector.

(Error information format for every sector)

1 + 46 × 11 = 507byte is used in one sector.

Last cylinder
Head of 0 head, 1 sector

← 2nd sector - 6th sector are the same.

Counter
BIN

← [1byte 0~46]

Error code	Cylinder (L)	Cylinder (H)	Head	Sector	Year	Month	Day	Hour	Minute	Second
BIN	BIN	BIN	BIN	BIN	BCD	BCD	BCD	BCD	BCD	BCD

3-18. FDD Diagnostics

This is a test program that checks floppy disk drives.

(Do not use this program after performing a D-RAM test.)

1) FDD Check

① Description

A test file is opened on a floppy disk and data (256 bytes) of 00h - FFh is written four times on the disk before read and verification are performed.

② Display

After making sure the screen looks like this, insert a formatted FD (W/R-TEST disk) into the drive and press any key.

```
Please insert W/R-TEST disk to drive A:

Warning
Data in the disk A: will be destroyed.
```

Note: The hatched drive name is [A:] or [B:].
W/R-TEST disk: Formatted FD (Turn off write-protection)

The screen looks like this during testing.

```
FDD Write/Read & Compare Check
```

③ Error

When an error occurs, the following message appears on screen.

```
**********
**********  FDD ERROR !!!  **********
 Drive not ready
```

Note: An error message appears at the hatched area

Error message	Description
Drive not ready	No FD in drive
Verify error	Write data is different from Read data
Write protect error	Disk is write-protected.
General failure	FD is not formatted or others
No space left on device	No disk space available

Other than those message, some MS-DOS error message may be displayed.

④ Terminating testing

When the screen displays the following message, remove the FD and press any key.

```
Please out W/R-TEST disk from drive A:
```

Note: The hatched area is the drive name [A:] or [B:].

3-19. Fan & LCD ON/OFF Diagnostics

1) Fan & LCD ON/OFF Check

① Checking content

The CPU, the fan, the exhaust fan and the LCD are turned ON/OFF.

When this menu is selected, the following display is shown.

```
FAN&LCD ON/OFF Diagnostics

HIT ANY KEY
```

When any key is pressed, "1" is written to bit 4 of PSC2 general use I/O port HIOP. At that time, the CPU fan and the exhaust fan are stopped and the LCD and the backlight are turned off.

When any key is pressed under this state, or if there is no key input for 10 sec, the display automatically returns to the main menu and the test is terminated.

When the system exits this diagnostic job, "0" is written to HIOP bit 4.

3-20. Power Hold Diagnastics

1) Power Hold Check

① Checking content

Two types of states such as power hold and power switch are displayed.

```
Power Hold Diagnostics
      Power Hold   : ON (or OFF)
      Power Switch : ON (or OFF)
```

When pressing the space key, bit 5 of PSC2's general I/O port HIOP is inverted, and power hold is switched between ON and OFF.

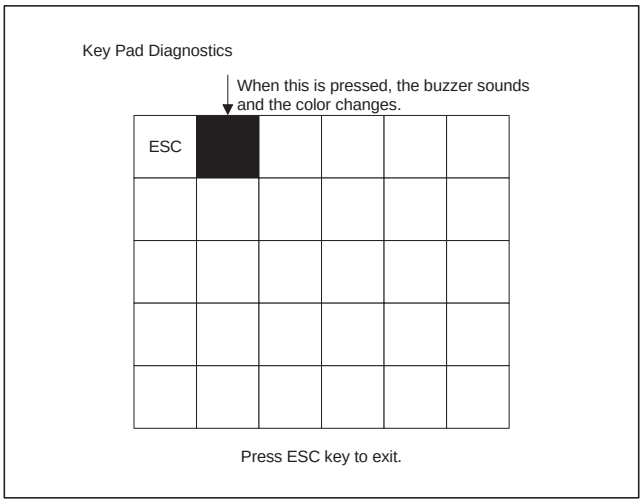
In addition, bit 1 of PSC2's general port HIOP is read at every 200ms. Power Switch: OFF is displayed when this bit is "0", and Power Switch: ON is displayed when this bit is "1".

3-21 Key Pad Diagnostics

1) Key Pad Check

The UP-C30PK key test is performed. In the UP-C30PK, keys are detected by matrix scan of KBC (M38802M270).

① Display



② Content

When a key is pressed, its color changes and the key catch sound is made.

The keys to be checked and their positions are as shown below.

ESC	F4	F5	F10	Delete	Back Space
7	8	9	Tab	↑	↓
4	5	6	L-Shift	←	→
1	2	3	L-Ctrl	Space	
0		•	L-Alt	Enter	

③ End

Press the ESC key to terminate the test.

CHAPTER 5. CIRCUIT DESCRIPTION

1.

1-1. CPU

Pentium Processor: A80502CSLM66133SY028

- External Bus Interface: 66MHz
- L1 cache: 8K Code & 8K Data (Writeback) cache
- 64-Bit Data Bus

1-2. Chipset

FireStar Plus: 82C700U3.2

- PCI Bus:
- DRAM controller (FPM, EDO or SDRAM): FPM or EDO supported
- ISA Bus: AT Clock = 8.33MHz
- Bus Mastering IDE: Primary IDE supported, Not Secondary
- Thermal Management: Not used
- Unified Memory Management (UMA):
- DMA controller: 8237A × 2
- Interval Timer: 8254
- Interrupt controller: 8259 × 2

1-3. PS/2 Keyboard Controller

KBC: M38802M270

- Full keyboard control
- Mouse control: Not used
- Matrix Key control: Not used

1-4. Graphic Controller

VGAC: MN89305

- XGA compatible
- LCD (640 × 480 × 256/64k color; 800 × 600 × 256/64k color; 024 × 768 × 256 color) control
- Host intrface: PCI/ISA/I386/I486/VL interface (Used for PCI interfce)
- DRAM interface: 4M DRAM (16-bit) × 1or2, 16M DRAM (16-bit) × 1or2
- Vcc=3.3V only

1-5. Super I/O Controller

M5113A2

- FDC: Disable
- Serial Port: 16C550 compatible with Infrared × 2
- Parallel Port: used for LPT1

1-6. System Controller 2

PSC2: LZ9AM22

- BIOS ROM Bank Control: Fixed 2banks
- Mask ROM Bank Control: Fixed 256banks
- Flash ROM Bank Control: Max. 384banks
- PS-RAM Bank Control: Max. 192banks
- UART × 5: COM 5ch
- Clocked Serial I/O × 2: CKDC VII I/F (Not used)
- Mode Switch Sense: 16bits (Not used)
- Clerk Switch Sense: 16bits (Not used)
- MCR I/F: 2track
- Drawer I/F: 2drawers

1-7. Memory

- L2 cache: None
- System Memory: DRAM Standard = 1M × 16b EDO Asym 60ns Vcc = 3.3V × 4chip (8MB)
  Option = 144pin S.O.DIMM socket × 1 (8MB/16MB/32MB)
- BIOS ROM: 512K × 8b (512KB) Flash ROM
  Vcc = 5.0V
- DOS ROM: 1M × 16b (2MB) Mask ROM
  Vcc = 5.0V
- Flash ROM Disk: Standard = 1M × 16b (2MB)
  Vcc = 5.0V
  Option = 2M × 16b (4MB)
- PS-RAM Disk: Standard = 512K × 8b × 2chip (1MB)
  Vcc = 3.3V
  Option = 512K × 8b × 4chip (2MB)
- Video RAM: 256K × 16b × 2chip (1MB)
  Vcc = 3.3V

1-8. Analog Touch Panel

- Controller: N010-0559-V021
- RS-232C I/F (2400/4800/9600bps):
  used for 9600bps
- Resolution: 1024 × 1024

1-9. LCD

- Color LCD: 10.4" DSTN 640 × 480 × 256color

1-10. System Switch

- DIP Switch: 8circuits
- Jumper Switch: Not used
- 0Ω Register: Not used

1-11. Serial Ports

- Serial 1 (Used for COM1): Ci/+5V switchable – DSUB9 with FIFO (by Super I/O)
- Serial 2 (Used for COM2): Ci/+5V switchable – DSUB9 with FIFO (by Super I/O)
- Serial 3 (Used for COM3/5): SG/+5V Pattern-cut & Jumper – RJ45 without FIFO (by PSC2)
- Serial 4 (Used for COM4/6): – RJ45 without FIFO (by PSC2)
- Serial 5: Used for Built-in printer – TTL level interface
- Serial 6: Used for Customer VFD control – RJ45(for UP-P20DP) or 7pin-CN(for UP-I20DP)
- Serial 7: Used for Touch panel control – TTL level interface

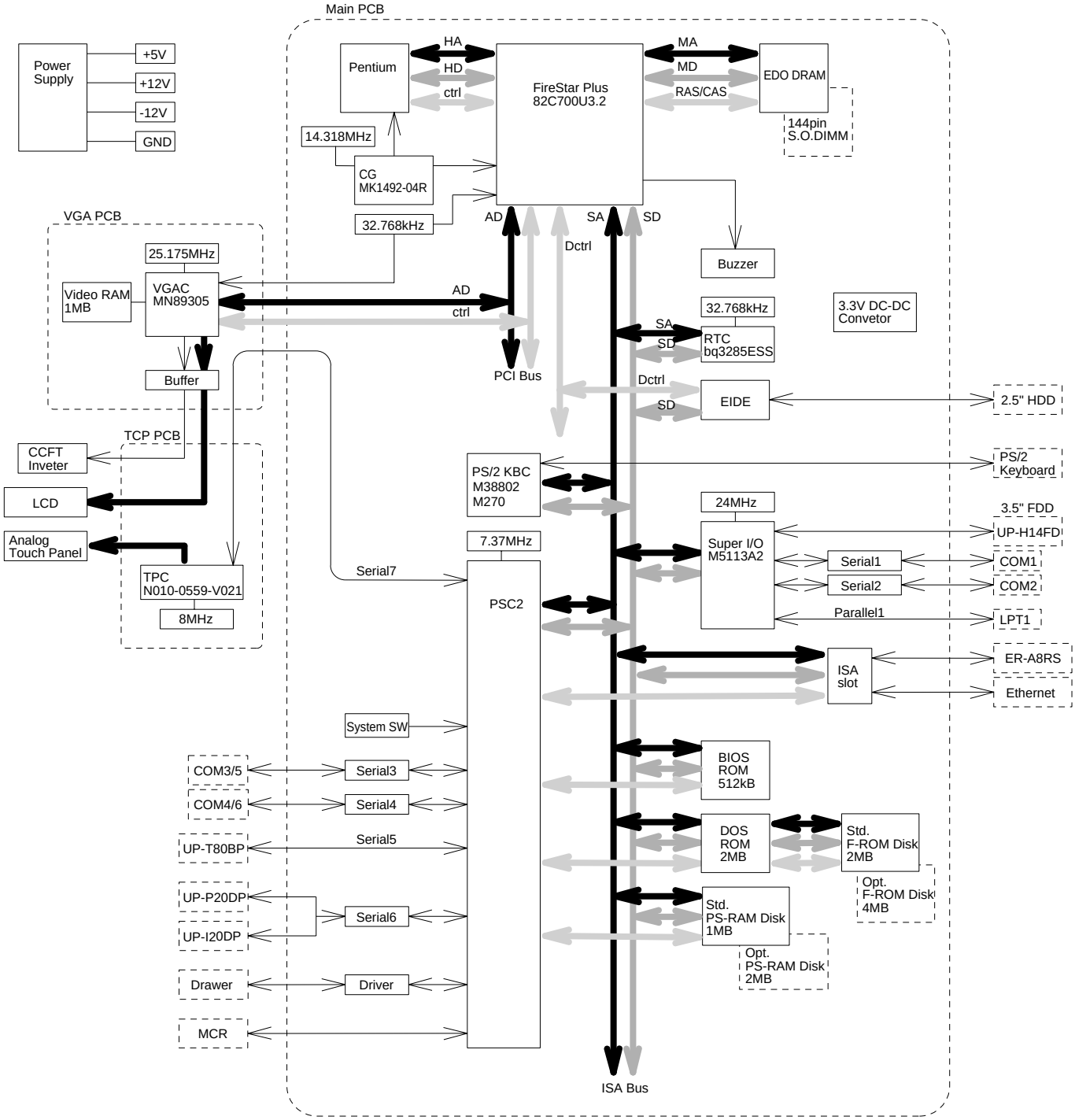
1-12. Power Supply Unit

- Input = AC220 - 240V, 50/60Hz

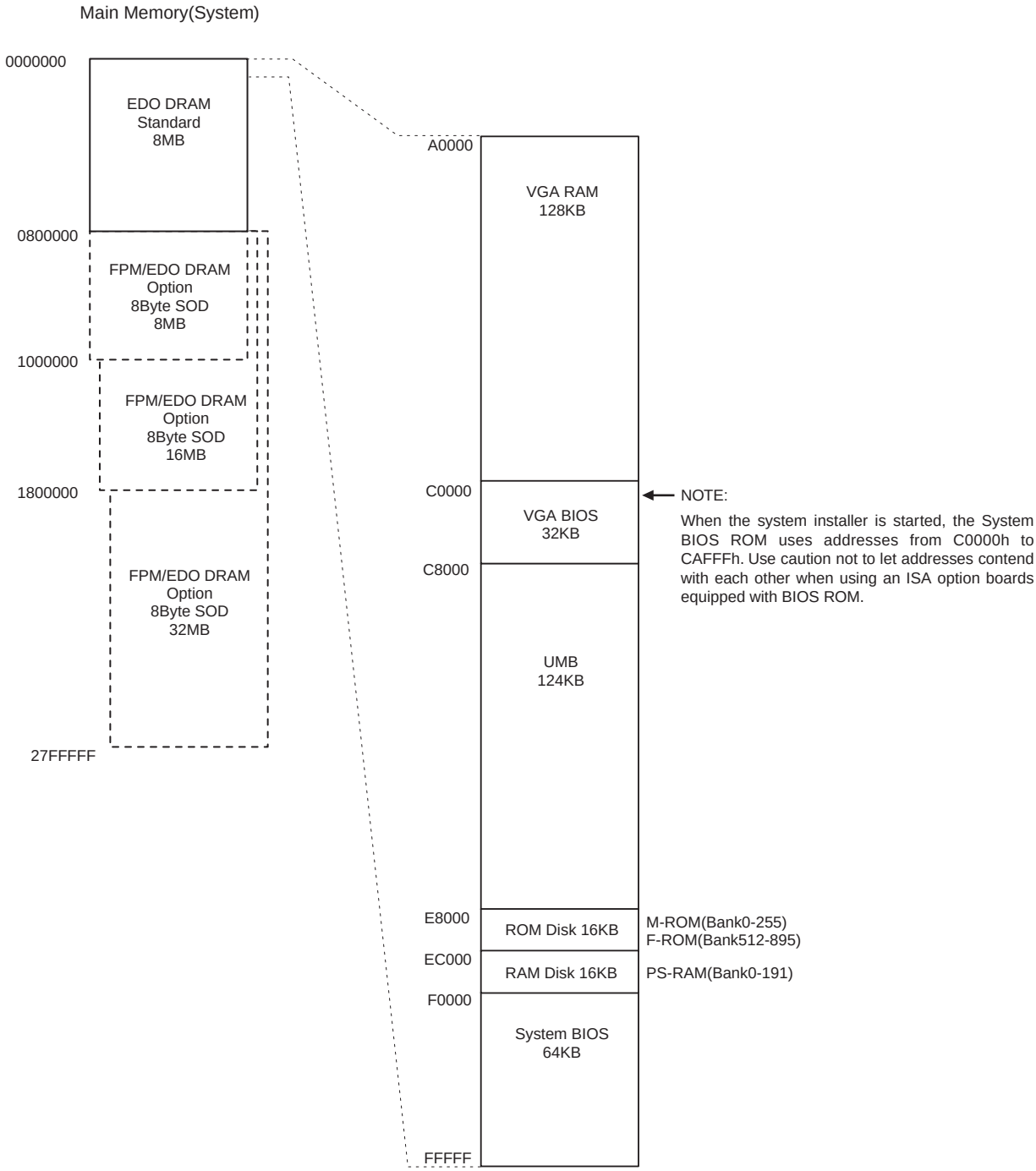
1-13. Vacuum Fluorescent Display Unit: 202MD11AB (used Pole display unit: UP-P20DP/i20DP)

- VFD = 20 Digits × 2 Lines, 5 × 7dots with; (Period & Comma) + 20 ▽
- Microcontroller with Character Generator
- RS-232C I/F (RXD/DSR/DTR,4800/9600/19200/38400bps):
  used for 9600bps
- Power: +5VDC/1A
- Auto indicator blinking: When power is turn on, automatically blink the indicator of 1st digit.

2. Block Diagram



3. Memory Map


Main Memory(System)
0000000
EDO DRAM
Standard
8MB
0800000
FPM/EDO DRAM
Option
8Byte SOD
8MB
1000000
FPM/EDO DRAM
Option
8Byte SOD
16MB
1800000
FPM/EDO DRAM
Option
8Byte SOD
32MB
27FFFFF
A0000
VGA RAM
128KB
C0000
VGA BIOS
32KB
C8000
UMB
124KB
E8000
ROM Disk 16KB
M-ROM(Bank0-255)
F-ROM(Bank512-895)
EC000
RAM Disk 16KB
PS-RAM(Bank0-191)
F0000
System BIOS
64KB
FFFFF
NOTE:
When the system installer is started, the System BIOS ROM uses addresses from C0000h to CAFFFh. Use caution not to let addresses contend with each other when using an ISA option boards equipped with BIOS ROM.

4. I/O Address Map

4-1. PC specification

Address	Legacy ISA I/O
00-0F	DMA ch0-3 control
10- 1F	(System)
20- 21	Master 8259 Interrupt control
22- 24	Chipset Configuration
40- 43	Timer control
48- 4B	(Timer control)
50-52	(System)
60- 6F	Keyboard/Mouse control
70- 7F	RTC/CMOS RAM Index/Data
80- 8F	DMA Page Register
90- 9F	System Port A Register (PS/2 port)
A0-A1	Slave 8259 Interrupt control
C0-DE	DMA ch4-7 control
F0- F1	(Coprocessor busy clear/reset)
102	65550(VGAC) Global Enable Register
110-16F	
170-177	Secondary IDE control
180-19F	POS I/O
1A0-1EF	
1F0-1F7	Primary IDE control
200-26F	
278-27F	[Parallel Port 2 (LPT2) control]
280-2DF	
2E8-2EF	COM4 control
2F0-2F7	
2F8-2FF	COM2 control
300-36F	
378-37F	Parallel Port 1 (LPT1) control
380-38F	
398	Super I/O Configuration Port
3A0-3AF	
3BC-3BF	[Parallel Port 3 (LPT3) control]
3C0-3DF	EGA/VGA control
3E0-3E4	PCIC PCMCIA controllers
3E5	[BIOS ROM Write Control]
3E8-3EF	COM3 control
3F0-3F7	FD/HD control
3F8-3FF	COM1 control
400-40A	
40B	EISA DMA Extended Mode control
410-4EF	
4D6	EISA DMA Extended Mode control
4D7-57F	
580-59F	POS I/O
5A0-7EF	
7F0-7F1	PSC Special System Register
7F2-7FF	
800-97F	
980-99F	POS I/O
9A0-A78	
A79	[(PnP ISA Auto Configuration Port)]
A7A-BFF	
C00-CF7	
CF8-CFF	PCI Configuration
D00-D7F	
D80-D9F	Reserved [POS I/O]
DA0-FFF	

4-2. POS specification

Address	POS I/O	UP-5300 U/A
180-189	Extended Interrupt control	○
18A	Drawer control	○
18B-18F	Timer Counter control	○
190-191	CSIO1 (CKDC) control	Reserved
192-193	CSIO2 (CKDC) control	Reserved
194	BIOS Bank control	○
195	ROM & RAM Disk Base Address	○
196-197	Interrupt Status Read	○
198-199	Mask/Flash ROM Bank control	○
19A-19B	PS-RAM Bank control	○
19C-19D	Mode Switch	Reserved
19E-19F	Clerk Switch	Reserved
580-585	MCR control	○
588	General Purpose I/O	○
590-597	COM5 (Serial3) control	○
598-59F	COM6 (Serial4) control	○
980-987	Serial5 (Built-in Printer)	○
988-98F	Serial6 (CU.VFD) control	○
990-997	Serial7 (Touch Panel) control	○
D80-D8F	[Option]	
D90-D9F	[Option]	

5. DMA Channel Mapping

DMA Channel	Legacy ISA DMA function
0	ISA Expansion
1	—
2	Floppy Disk Controller
3	ECP parallel port on LPT1
4	[Cascade]
5	—
6	—
7	—

6. IRQ

6-1. IRQ Mapping list

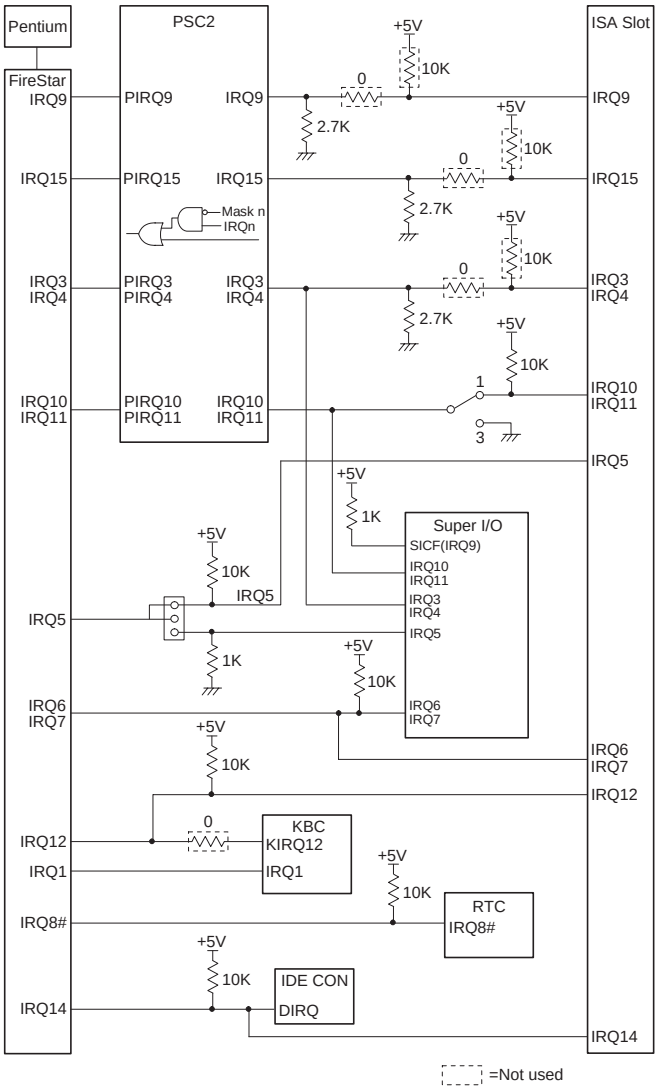
Controller1 8259	Controller2 8259	Fixed ISA Default	Power On Default	Available Device	UP-5x00 Recommended
IRQ0		System timer	Timer	Timer	Timer
IRQ1		Keyboard	KBC	KBC	KBC
IRQ2		PIC cascade	(Cascade)	(Cascade)	×
	IRQ8	RTC/CMOS	RTC/CMOS	RTC/COMS	RTC/CMOS
	IRQ9	—	IRQx	IRQx	IRQx
	IRQ10	(COM4)	ISA/Serial4	Serial4/3/7/ISA	COM4†
	IRQ11	(COM3)	ISA/Serial3	Serial3/4/7/ISA	COM3†
	IRQ12	Mouse	ISA/[KBC]	ISA/[KBC]	SRN/Ethernet
	IRQ13	Coprocessor	×	×	×
	IRQ14	Primary IDE	HDC	HDC	HDC
	IRQ15	Secondary IDE	Serial7	Serial7/3/4/IRQx	Touch Panel
IRQ3		COM2	Serial2	Serial2	COM2
		COM4	×/Serial4	×/Serial4	×
IRQ4		COM1	Serial1	Serial1	COM1
		COM3	×/Serial3	×/Serial3	×
IRQ5		(LPT2)	ISA	ISA	LPT2†
IRQ6		FDC	FDC	FDC	FDC
IRQ7		LPT1	LPT1	LPT1	LPT1

† = ER-A8RS(Serial 2ch & Parallel 1ch) may be used.

[ ] = This function is used with 0ohm Resistor, etc.

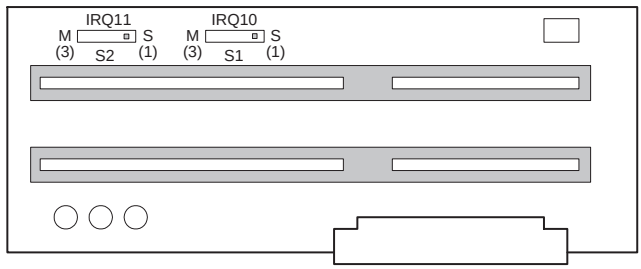
Extended Interrupt	On-Board POS Device
IRQx0	MCR (UP-E12MR2)
IRQx1	Serial5 [Built-in Printer] UP-T80BP
IRQx2	Serial6 [VFD] UP-P20DP/I20DP
IRQx3	POS Key (Not used)
IRQx4	CSIO1 I/F (Not used)
IRQx5	CSIO2 I/F (Not used)
IRQx6	FROM Busy
IRQx7	POFF
IRQx8	SINT0
IRQx9	Reserved [Mode Switch] (Not used)
IRQx10	TC0OVF
IRQx11	TC0CMP
IRQx12	TC1CMP
IRQx13	Serial4 (COM6)
IRQx14	Serial3 (COM5)
IRQx15	Clerk Switch (Not used)

6-2. IRQ Block Chart



6-3 IRQ Switch

Riser board (parts side)



S1 = IRQ10: S(1) = ON (Connect IRQ10 to the ISA Slot.)
M(3) = OFF (Connect IRQ10 to GND, not to the ISA Slot.)

S2 = IRQ11: S(1) = ON (Connect IRQ11 to the ISA Slot.)
M(3) = OFF (Connect IRQ11 to GND, not to the ISASlot.)

7. CPU

7-1. Introduction

Intel's Pentium Processor (A80502CSLM66133SY028) is used.

Pentium Processor Bus Frequency Selection

Core Frequency (max)	External Bus Frequency (max)	Bus/Core Ratio	BF1 (Y33)	BF0 (Y35)	Selection
100MHz	66MHz	2/3	1	1	UP-5300 Setting

Setting 1 = 10kohm Pull up (Vcc3)
0 = 0ohm Grounding

MicroClock MK1492-04R Power-up Input Setting

Pin #	Name	Internal Resistor	Setting	Function
5	OE	Mid-level	Default	All Clock Outputs Enabled
15	CPUS#	Pull up	Default	
16	PCISTP#	Pull up	Default	HOST = 66.66MHz
24	FS	Pull up	Default	
27	CSSS	Pull up	Default	Power Down Mode = All Clocks On
19	DS	Pull up	Default	HOST7,8 Tristated
21	SEL0	Pull up	Default	48M/14.3M = 48.0MHz
22	LE	Pull up	Pull down	EMI Control ON
25	SEL1	Mid-level	Default	F1 = 14.318MHz
28	PEN	Mid-level	Default	Pin25 = PCI, Pin24=PCIF

The external pull down resistor is 10kohm.

MicroClock MK1492-04R Clock Output

Pin #	Name	Condition
5	14.3	14.318MHz for FireStar
8	EHOST1	Early CPU Clock for FireStar
10	HOST2	CPU Clock for Pentium
12	HOST3	Not used (Host Output Clock)
13	HOST4	Not used (Host Output Clock)
18	HOST5,7	Not used (Host Output Clock)
19	HOST6,8	Not used (Host Output Clock)
21	48M/14.3M	Not used (48.0MHz Clock)
22	PCIF	Not used (PCI Clock)
24	PCI	Not used (PCI Clock)
25	PCI	Not used (PCI Clock)
27	PCI	PCI Clock for FireStar
28	F1	Not used (14.318MHz Clock)

7-2. Pin assignments

7-3. Pin description

Table 4. Quick Pin Reference

Symbol	Type	Name and Function
A20M#	I	When the address bit 20 mask pin is asserted, the Pentium processor emulates the address wrap around at 1 Mbyte which occurs on the 8086. When A20M# is asserted, the processor masks physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode.
A31-A3	I/O	As outputs, the address lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31-A5.
ADS#	O	The address status indicates that a new valid bus cycle is currently being driven by the processor.
AHOLD	I	In response to the assertion of address hold, the processor will stop driving the address lines (A31-A3), and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles.
AP	I/O	Address parity is driven by the processor with even parity information on all processor generated cycles in the same clock that the address is driven. Even parity must be driven back to the processor during inquire cycles on this pin in the same clock as EADS# to ensure that correct parity check status is indicated.
APCHK#	O	The address parity check status pin is asserted two clocks after EADS# is sampled active if the processor has detected a parity error on the address bus during inquire cycles. APCHK# will remain active for one clock each time a parity error is detected.
BE7#-BE5# BE4#-BE0#	O I/O	The byte enable pins are used to determine which bytes must be written to extemal memory, or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A31-3).
BF [1:0]	I	Bus Frequency determines the bus-to-core ratio. BF [1:0] is sampled at RESET, and cannot be changed until another non-warm (1 ms) assertion of RESET. Additionally, BF [1:0] must not change values while RESET is active.
BOFF#	I	The backoff input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the processor will float all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time the Pentium processor restarts the aborted bus cycle(s) in their entirety.
BP [3:2] PM/BP [1:0]	O	The breakpoint pins (BP3-0) correspond to the debug registers, DR3-DR0. These pins extemally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the performance monitoring pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
BRDY#	I	The burst ready input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the processor data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.
BREQ	O	The bus request output indicates to the extemal system that the processor has internally generated a bus request. This signal is always driven whether or not the processor is driving its bus.
BUSCHK#	I	The bus check input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the processor will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the processor will vector to the machine check exception.
CACHE#	O	For processor-initiated cycles, the cache pin indicates internal cacheability of the cycle (if a read), and indicates a burst writeback cycle (if a write). If this pin is driven inactive during a read cycle, the processor will not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The clock input provides the fundamental timing for the processor. Its frequency is the operating frequency of the processor external bus and require TTL levels. All external timing parameters except TDI, TDO, TMS, TRST# and PICD0-1 are specified with respect to the rising edge of CLK. NOTE: It is recommended that CLK begin 150 ms after Vcc reaches its proper operating level. This recommendation is only to assure the long term reliability of the device.
D/C#	O	The data/code output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.
D63-D0	I/O	These are the 64 data lines for the processor. Lines D7-D0 define the least significant byte of the data bus; Lines D63-D56 define the most significant byte of the data bus. When the CPU is driving the data lines, they are driven during the T2, T12 or T2P clocks for that cycle. During reads, the CPU samples the data bus when BRDY# is returned.
DP7-DP0	I/O	These are the data parity pins for the processor. There is one for each byte of the data bus. They are driven by the processor with even parity information on writes in the same clock as write data. Even parity information must be driven back to the Pentium processor with voltage reduction technology on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the processor. DP7 applies to D63-D56; DP0 applies to D7-D0.
EADS#	I	This signal indicates that a valid external address has been driven onto the processor address pins to be used for an inquire cycle.
EWBE#	I	The external write buffer empty input, when inactive (high), indicates that a write cycle is pending in the extemal system. When the processor generates a write and EWBE# is sampled inactive, the processor will hold off all subsequent writes to all E-or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.
FERR#	O	The floating point error pin is driven active when an unmasked floating point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using DOS-type floating point error reporting.

Symbol	Type	Name and Function
FLUSH#	I	When asserted, the cache flush input forces the processor to write back all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle will be generated by the processor indicating completion of the writeback and invalidation. NOTE: If FLUSH# is sampled low when RESET transitions from high to low, tristate test mode is entered.
HIT#	O	The hit indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either the data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.
HITM#	O	The hit to a modified line output is driven to reflect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HLDA	O	The bus hold acknowledge pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the processor has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and the processor will resume driving the bus. If the processor has a bus cycle pending, it will be driven in the same clock that HLDA is de-asserted.
HOLD	I	In response to the bus hold request, the processor will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The processor will maintain its bus in this state until HOLD is de-asserted. HOLD is not recognized during LOCK cycles. The processor will recognize HOLD during reset.
IERR#	O	The internal error pin is used to indicate internal parity errors. If a parity error occurs on a read from an internal array, the processor will assert the IERR# pin for one clock and then shutdown.
IGNNE#	I	This is the ignore numeric error input. This pin has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0, and the IGNNE# pin is asserted, the processor will ignore any pending unmasked numeric exception and continue executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the processor will execute the instruction in spite of the pending exception. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the processor will stop execution and wait for an external interrupt.
INIT	I	The processor initialization input pin forces the processor to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power up. If INIT is sampled high when RESET transitions from high to low, the processor will perform built-in self test prior to the start of program execution.
INTR	I	An active maskable interrupt input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the processor will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to assure that the interrupt is recognized.
INV	I	The invalidation input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock EADS# is sampled active.
KEN#	I	The cache enable pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the processor generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle will be transformed into a burst line fill cycle.
LOCK#	O	The bus lock pin indicates that the current bus cycle is locked. The processor will not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be de-asserted for at least one clock between back-to-back locked cycles.
M/IO#	O	The memory/input-output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
NA#	I	An active next address input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The processor will issue ADS# for a pending cycle two clocks after NA# is asserted. The processor supports up to two outstanding bus cycles.
NMI	I	The non-maskable interrupt request signal indicates that an extemal non-maskable interrupt has been generated.
PCD	O	The page cache disable pin reflects the state of the PCD bit in CR3; Page Directory Entry or Page Table Entry. The purpose of PCD is to provide an extemal cacheability indication on a page-by page basis.
PCHK#	O	The parity check output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned.
PEN#	I	The parity enable input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock, a data parity error is detected. The processor will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to "1", the processor will vector to the machine check exception before the beginning of the next instruction.
PM/BP[1:0]	O	These pins function as part of the performance monitoring feature. The breakpoint 1-0 pins are multiplexed with the performance monitoring 1-0 pins. The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.

Symbol	Type	Name and Function
PRDY	O	The probe ready output pin indicates that the processor has stopped normal execution in response to the R/S# pin going active or Probe Mode being entered.
PWT	O	The page write-through pin reflects the state of the PWT bit in CR3, the page directory entry, or the page table entry. The PWT pin is used to provide and extemal writeback indication on a page-by-page basis.
R/S#	I	The run/stop input is an asynchronous, edge-sensitive interrupt used to stop the normal execution of the processor and place it into an idle state. A high to low transition on the R/S# pin will interrupt the processor and cause it to stop execution at the next instruction boundary.
RESET	I	RESET forces the processor to begin execution at a known state. All the processor internal caches will by invalidated upon the RESET. Modified lines in the data cache are not written back. FLUSH# and INIT are sampled when RESET transitions from high to low to determine if tristate test mode will be entered or if BIST will be run.
SCYC	O	The split cycle output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are locked.
SMI#	I	The system management interrupt causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACT#	O	An active system management interrupt active output indicates that the processor is operating in System Management Mode.
STPCLK#	I	Assertion of the stop clock input signifies a request to stop the internal clock of the Pentium processor with voltage reduction technology thereby causing the core to consume less power. When the CPU recognizes STPCLK#, the processor will stop execution ont eh next instruction boundary, unless superseded by a higher priority interrupt, and generate a Stop Grant Acknowledge cycle. When STPCLK# is asserted, the processor will still respond to extemal snoop requests.
TCK	I	The testability clock input provides the clocking function for the processor boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the processor during boundary scan.
TDI	I	The test data input is a serial input for the test logic. TAP instructions and data are shifted into the processor on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O	The test data output is a serial output of the test logic. TAP instructions and data are shifted out of the processor on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the test mode select input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the test reset input allows the TAP controller to be asynchronously initialized.
Vcc2	I	These pins are the 2.9V (3.1V for 150 MHz) power inputs to the Pentium processor with voltage reduction technology.
Vcc3	I	These pins are 3.3V power inputs to the Pentium processor with voltage reduction technology.
Vss	I	These pins are the ground inputs to the Pentium processor with voltage reduction technology.
W/R#	O	Write/read is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The writeback/writethrough input allows a data cache line to be defined as writeback or writethrough on a line-by-line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

8. Chipset

8-1. Introduction

OPTi's FireStar Plus (82C700U3.2) is used.

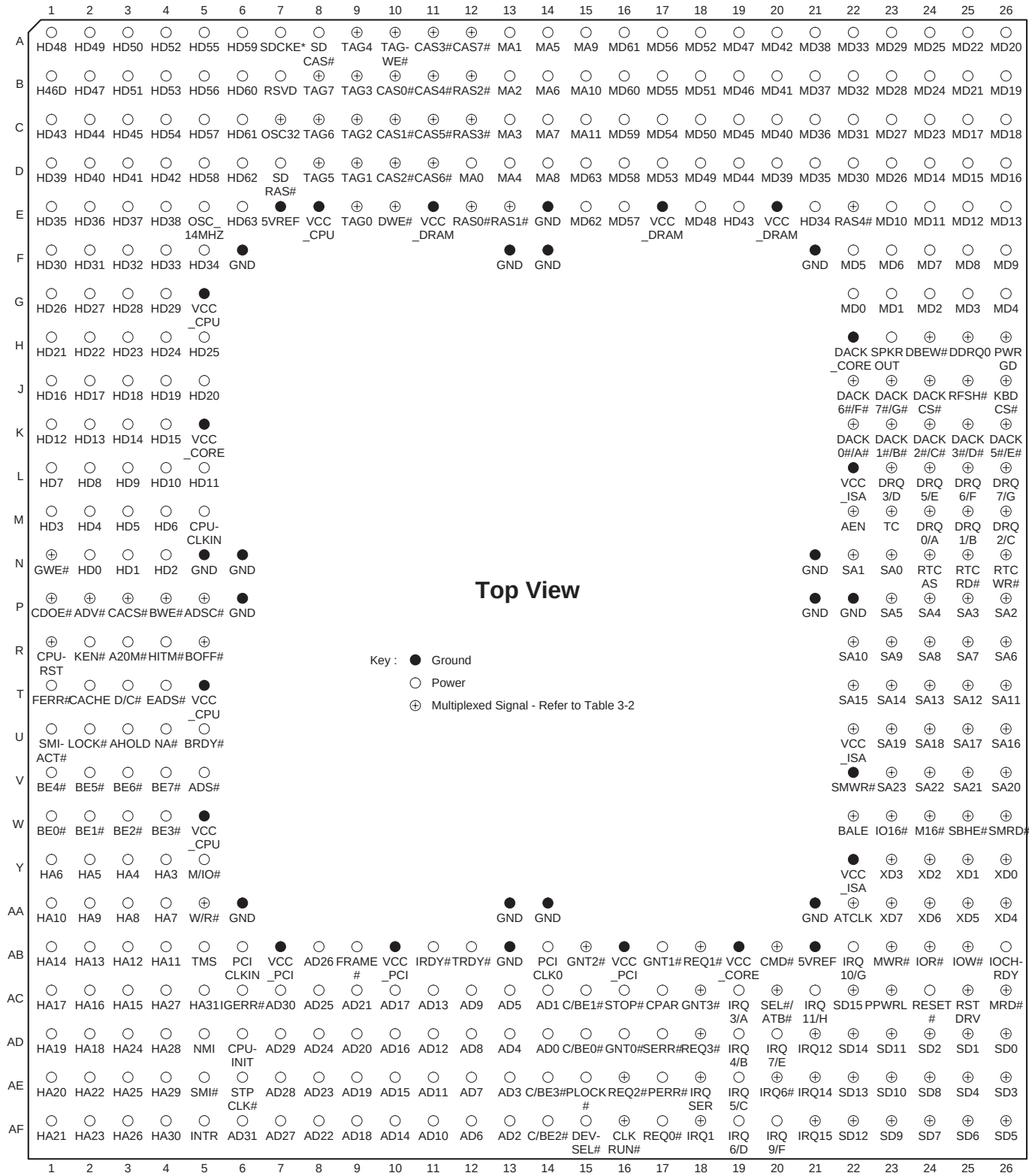
FireSter Strap Options

Pin No.	Pin Name	Internally at Reset	Setting	Function
N25	RTCRD#	Pull low	Pull high (Vcc5)	PCICLK1 Enable
N26	RTCWR#	Pull low	Pull low	PCICLK2 Disable
J24	ROMCS#	Pull low	Pull low	PCICLK3-5 Disable
J26	KBDCS#	Pull low	Pull low	
AF5	INTR	Pull high	Pull high	PCIVCC = 3.3V
AD5	NMI	Pull high	Pull high	DRAMVCC = 3.3V
AC6	IGERR#	Pull low	Pull low	ISAVCC = 5.0V
H24	DBEW#	Pull low	Pull low	PPWR = Normal mode
R5	BOFF#	Pull low	Pull low	PPWR0# Selected
N24	RTCAS	Pull high	Pull low	Normal decode ISA mode
R3	A20M#	Pull high	Pull high (Vcc3)	
AB14	PCICLK0	Pull low	Pull low	No MCACHE support
B7	RSVD	Pull low	Pull low	CPUVCC = 3.3V

The internal resister is about 50 kohm.

The external resister is 10 kohm.

8-2. Pin assignments



Note: *In FireStar ACPI pin A7 becomes SDCKE, where as in the non~ACPI version it is reserved. However, in both versions pin A7 is still used as part of the input address for NAND tree test mode.

8-3. Pin description

8-3-1. CPU Interface Signals Set

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
Host Data Bus				
HD[63:0]	Refer to Table 3-2	I/O (4mA)		**Host Data Bus Lines 63 through 0:** Provides a 64-bit data path to the CPU.
CPU Address				
HA[31:3]	Refer to Table 3-2	I/O (4mA)		**Host Address Bus Lines 31 through 3:** HA[31:3] are the address lines of the CPU bus. HA[31:3] are connected to CPU lines A[31:3]. Along with the byte enable signals, HA[31:3] define the physical area of memory or I/O being accessed. During CPU cycles, the HA[31:3] lines are inputs. They are used for address decoding and second level cache tag lookup sequences. During inquire cycles, the HA[31:5] lines are outputs to the CPU to snoop the first level cache tags. They also are outputs to the L2 cache.
BE[7:0]#	V4:V1, W4:W1	I		**Byte Enables 7 through 0:** Selects the active byte lanes on HD[63:0].
NMI	AD5 Strap option pin, refer to Table 3-7	O (4mA)		**Non-Maskable Interrupt:** This signal is activated when a parity error from a local memory read is detected or when the IOCHK# signal from the ISA bus is asserted and the corresponding control bit in Port B is also enabled.
INTR	AF5 Strap option pin, refer to Table 3-7	O (4mA)		**Interrupt Request:** INTR is driven to signal the CPU that an interrupt request is pending and needs to be serviced. The interrupt controller must be programmed following a reset to ensure that INTR is at a known state.
FERR#	T1	I		**Floating Point Coprocessor Error:** This input causes two operations to occur. IRQ13 is triggered and IGERR# is enabled. An I/O write to Port F0h will set IGERR# low when FERR# is low.
IGERR#	AC6 Strap option pin, refer to Table 3-7	I/O (4mA)		**Ignore Coprocessor Error:** Normally high, IGERR# will go low after FERR# goes low and an I/O write to Port 0F0h occurs. When FERR# goes high, IGERR# is driven high.
CPU Control/Status				
CPUINIT	AD6	O		**CPU Initialize:** a shutdown cycle or a low-to-high transition of I/O Port 092h bit 0 will trigger CPUINIT. If keyboard emulation is enabled (default), a CPUINIT will be generated when a Port 064h write cycle with data FEh is decoded. If keyboard emulation has been disabled, then this signal will be triggered when it sees the KBRST from the keyboard.
M/IO#	Y5	I		**Memory/Input-Output:** M/IO#, D/C#, and W/R# define CPU bus cycles. Interrupt acknowledge cycles are forwarded to the PCI bus as PCI interrupt acknowledge cycles. All I/O cycles and any memory cycles that are not directed to memory controlled by the DRAM interface are forwarded to PCI.
D/C#	T3	I		**Data/Control:** D/C#, M/IO#, and W/R# define CPU bus cycles. (See M/IO# definition above.)
W/R#	AA5	I/O (4mA)	Cycle Multiplexed	**Write/Read:** W/R#, D/C#, and M/IO# define CPU bus cycles. (See M/IO# definition above.)
INV		O (4mA)		**Invalidate:** Pin AA5 also serves as an output signal and is used as INV for L1 cache during an inquire cycle.
ADS3	V5	I		**Address Strobe:** The CPU asserts ADS# to indicate that a new bus cycle is beginning. ADS# is driven active in the same clock as the address, byte enables, and cycle definition signals. ADS# has an internal pull-up resistor that is disabled when the system is in the Suspend mode.
BRDY#	U5	O (4mA)		**Burst Ready:** BRDY# indicates that the system has responded in one of three ways: 1) Valid data has been placed on the CPU data bus in response to a read, 2) CPU write data has been accepted by the system, or 3) the system has responded to a special cycle.

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
NA#	U4	O (4mA)		**Next Address:** This signal is connected to the CPU's NA# pin to request pipelined addressing for local memory cycle. FireStar asserts NA# for one clock when the system is ready to accept a new address from the CPU, even if all data transfers for the current cycle have not completed.
KEN#	R2	O (4mA)		**Cache Enable:** This pin is connected to the KEN# input of the CPU and is used to determine whether the current cycle is cacheable.
EADS#	T4	O (4mA)	Cycle Multiplexed	**External Address Strobe:** This output indicates that a valid address has been driven onto the CPU address bus by an external device. This address will be used to perform an internal cache inquiry cycle when the CPU samples EADS# active.
WB/WT#				**Writeback/Write-Through:** Pin T4 is also used to control writeback or write-though policy for the primary cache during CPU cycles.
HITM#	R4	I		**Hit Modified:** Indicates that the CPU has had a hit on modified line in its internal cache during an inquire cycle. It is used to prepare for writeback.
CACHE#	T2	I		**Cacheability:** This input is connected to the CACHE# pin of the CPU. It goes active during a CPU initiated cycle to indicate when, an internal cacheable read cycle or a burst writeback cycle, occurs.
AHOLD	U3	O (4mA)		**Address Hold:** This signal is used to tristate the CPU address bus for internal cache snooping.
LOCK#	U2	I		**CPU Bus Lock:** The processor asserts LOCK# to indicate the current bus cycle is locked. It is used to generate PLOCK# for the PCI bus. LOCK# has an internal pull-down resistor that is engaged when HLDA is active.
BOFF#	R5 Strap option pin, refer to Table 3-7	O (4mA)		**Back-off:** This pin is connected to the BOFF# input of the CPU.
CPURST	R1	O (4mA)	(Always)	**CPU Reset:** This signal generates a hard reset to the CPU whenever the PWRGD input goes active.
RSMRST			SYSCFG ADh[5] = 1	**Resume Reset:** Generates a hard reset to the CPU on resuming from Suspend mode.
Host Power Control				
SMI#	AE5	O (4mA)		**System Management Interrupt:** This signal is used to request System Management Mode (SMM) operation.
SMIACT#	U1	I		**System Management Interrupt Active:** The CPU asserts SMIACT# in response to the SMI# signal to indicate that it is operating in System Management Mode (SMM).
STPCLK#	AE6	O (4mA)		**Stop Clock:** This signal is connected to the STPCLK# input of the CPU. It causes the CPU to get into the STPGENT# state.
L2 Cache Control				
CDOE#	P1	O (4mA)	PCIDV1 80h = 00h	**Cache Output Enable:** This signal is connected to the output enables of the SRAMs of the L2 cache in both banks to enable data read.
CACS#	P3	O (4mA)	See SYSCFG 16h[7,5] bit descriptions on page 266	**Cache Chip Select:** This pin is connected to the chip selects of the SRAMs in the L2 cache to enable data read/write operations. If not used, the CS# lines of the cache should be tied low.
DIRTY		I/O (4mA)		**Tag Dirty Bit:** This separate dirty bit allows the tag data to be 8 bits wide instead of 7. DIRTY is a 5.0V tolerant input, even when its power plane is connected to 3.3V as long as the 5VREF pins of FireStar are connected to +5.0V.
BWE#	P4	O (4mA)		**Byte Write Enable:** Write command to L2 cache indicating that only bytes selected by BE[7:0]# will be written.
GWE#	N1	O (4mA)	SYSCFG 19h[7] = 0	**Global Write Enable:** Write command to L2 cache indicating that all bytes will be written.
TAG0	E9	I/O (4mA)	SYSCFG 11h[3] = 0	**Tag RAM Data Bit 0:** This input signal becomes an output whenever TAGWE# is activated to write a new tag to the Tag RAM.
TAG1	D9	I/O (4mA)	SYSCFG 00h[5] = 0 11h[3] = 0	**Tag RAM Data Bit 1:** This input signal becomes an output whenever TAGWE# is activated to write a new tag to the Tag RAM.

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
TAG2	C9	I/O (4mA)	SYSCFG 00h[5] = 0 11h[3] = 0	**Tag RAM Data Bit 2:** This input signal becomes an output whenever TAGWE# is activated to write a new tag to the Tag RAM.
TAG3	B9	I/O (4mA)	SYSCFG 00h[5] = 0 11h[3] = 0	**Tag RAM Data Bit3:** This input signal becomes an output whenever TAGWE# is activated to write a new tag to the Tag RAM.
TAG4	A9	I/O (4mA)	SYSCFG 11[3] = 0	**Tag RAM Data Bit 4:** This input signal becomes an output whenever TAGWE# is activated to write a new tag to the Tag RAM.
TAG5	D8	I/O (4mA)	SYSCFG 11h[3] = 0	**Tag RAM Data Bit 5:** This input signal becomes an output whenever TAGWE# is activated to write a new tag to the Tag RAM.
TAG6	C8	I/O (4mA)	SYSCFG 11h[3] = 0	**Tag RAM Data Bit 6:** This input signal becomes an output whenever TAGWE# is activated to write a new tag to the Tag RAM.
TAG7	B8	I/O (4mA)	SYSCFG 11h[3] = 0	**Tag RAM Data Bit 7:** This input signal becomes an output whenever TAGWE# is activated to write a new tag to the Tag RAM.
TAGWE#	A10	O (4mA)	PCIDV1 81h = 00h	**Tag RAM Write Enable:** This control strobe is used to update the Tag RAM with the valid tag of the new cache line that replaces the current one during external cache read miss cycles.
ADSC#	P5	O (4mA)	PCIDV1 82h = 00h	**Controller Address Strobe:** For a synchronous L2 cache operation, this pin is connected to the ADSC# input of the synchronous SRAMs.
ADV#	P2	O (4mA)	PCIDV1 83h = 00h	**Advance Output:** For synchronous cache L2 operation, this pin becomes the advance output and is connected to the ADV# input of the synchronous SRAMs.

8-3-2. DRAM and PCI Interface Signal Set

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
DRAM Interface				
RAS0#m E12	E12	O (8/12mA)	Cycle Multiplexed	**Row Address Strobe 0:** Each RAS# signal corresponds to a unique DRAM bank. Depending on the kind of DRAM modules being used, this signal may or may not need to be buffered externally. This signal, however, should be connected to the corresponding DRAM RAS# line through a damping resistor.
SDCS0#				**SDRAM Chip Select Line 0:** Each SDCS# output corresponds to a unique SDRAM Bank. When active, the SDRAM will accept the command from FireStar. These outputs must be connected to the SDRAM banks through a damping resistor.
RAS1#	E13	O (8/12mA)	Cycle Multiplexed if PCIDV1 85h = 00h	**Row Address Strobe 1:** Refer to RAS0# signal description.
SDCS1#				**SDRAM Chip Select Line 1:** Refer to SDCS0# description.
RAS2#	B12	O (8/12mA)	Cycle Multiplexed if PCIDV1 84h = 00h	**Row Address Strobe 2:** Refer to RAS0# signal description.
SDCS2#				**SDRAM Chip Select Line 2:** Refer to SDCS0# description.
RAS3#	C12	O (8/12mA)	Cycle Multiplexed	**Row Address Strobe 3:** Refer to RAS0# signal description.
SDCS3#				**SDRAM Chip Select Line 3:** Refer to SDCS0# description.
RAS4#	E22	O (8/12mA)	SYSCFG 19h[3] = 1	**Row Address Strobe 4 (primary copy):** Refer to RAS0# signal description.
MA12			SYSCFG 19h[3] = 1 PCIDV1 53h[6:5] = 10	**Memory Address Bus Line 12**
CAS[7:0]#	A12, D11, C11, B11, A11, D10, C10, B10	O (8mA)	Cycle Multiplexed	**Column Address Strobe Lines 7 through 0 (primary copies):** The CAS[7:0]# outputs correspond to the eight bytes for each DRAM bank. Each DRAM bank has a 64-bit data bus. These signals are typically connected directly to the DRAM's CAS# inputs through a damping resistor.
SDDQM[7:0]#				**SDRAM Data Mask Control Bits 7 through 0:** During SDRAM read cycles, these outputs control whether the DRAM output buffers are driven on the MD bus or not. During SDRAM write cycles, these outputs control whether or not MD data will be written into the memory device.

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
SDCAS#	A8	O		**SDRAM Column Address Strobe (primary copy):** This output is part of the SDRAM command combination. This pin should be connected to the SDRAM through a damping resistor.
SDRAS#	D7	O		**SDAM Row Address Strobe (primary copy):** This output is part of the SDRAM command combination. This pin should be connected to the SDRAM through a damping resistor.
DWE#	E10	O (8mA)	Cycle Multiplexed	**DRAM Write Enable (primary copy):** This signal is the common write enable for all 64 bits of DRAM if either fast page mode or EDO DRAMs are used. This signal can be buffered externally before connection to the WE# input of the DRAMs.
SDWE#				**SDRAM Write Enable:** This output is the write enable signal for SDRAM.
MA[11:0]	Refer to Table 3-2	O (8/12mA)		**Memory Address Bus Lines 11 through 0:** Multiplexed row/column address lines to the DRAMs. Depending on the kind of DRAM modules being used, these signals may or may not need to be buffered externally. MA12 is optionally available instead of RAS3# or RAS4#.
MD[63:32]	Refer to Table 3-2	I/O (4mA)		**Higher Order Memory Data Bus:** These pins are connected directly to the higher order DRAM data bus.
MD[31:0]	Refer to Table 3-2	I/O (4mA)		**Lower Order Memory Data Bus:** These pins are connected directly to the lower order DRAM data bus.
PCI Bus Interface				
AD[31:0]	Refer to Table 3-2	I/O (PCI)		**PCI Address an Data:** AD[31:0] are bidirectional address and data lines for the PCI bus. The AD[31:0] signals sample or drive the address and data on the PCI bus.
C/BE[3:0]#	AE14, AF14, AC15, AD15	I/O (PCI)		**PCI Bus Command and Byte Enables:** During the address phase of a transaction, C/BE[3:0]# define the PCI command. During the data phase, C/BE[3:0]# are used as the PCI byte enables. The PCI commands indicate the current cycle type, and the PCI byte enables indicate which byte lanes carry meaningful data. FireStar drives C/BE# as an initiator of a PCI bus cycle and monitors C/BE[3:0]# as a target.
CPAR	AC17	I/O (PCI)		**Calculated Parity Signal:** PAR is "even" parity and is calculated on 36 bits - AD[31:0] plus C/BE[3:0]#. PAR is generated for address and data phases and is only guaranteed to be valid on the PCI clock after the corresponding address or data phase.
FRAME#	AB9	I/O (PCI)		**Cycle Frame:** FRAME# is driven by the current bus master to indicate the beginning and duration of an access. FRAME# is asserted to indicate that a bus transaction is beginning. FRAME# is an input when FireStar is the target and an output when it is the initiator.
IRDY#	AB11	I/O (PCI)		**Initiator Ready:** IRDY# indicates FireStar's ability, as an initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on each clock that both IRDY# and TRDY# are sampled asserted. IRDY# is an input to when FireStar is the target and an output when it is the initiator.
TRDY#	AB12	I/O (PCI)		**Target Ready:** TRDY# indicates FireStar's ability to complete the current data phase of the transaction. It is used in conjunction with IRDY#. A data phase is completed on each clock that TRDY# and IRDY# are both sampled asserted. TRDY# is an input when FireStar is the initiator and an output when it is the target.
DEVSEL#	AF15	I/O (PCI)		**Device Select:** FireStar asserts DEVSEL# to claim a PCI transaction. As an output, FireStar asserts DEVSEL# when it samples configuration cycles to the configuration registers. FireStar also asserts DEVSEL# when an internal IPC address is decoded. As an input, DEVSEL# indicates the response to a transaction. If no slave claims the cycle, FireStar will assert DEVSEL# to terminate the cycle.
STOP#	AC16	I/O (PCI)		**Stop:** STOP# indicates that FireStar, as a targent, is requesting a master to sotp the current transaction. As a master, STOP# causes FireStar to stop the current transaction. STOP# is an output when FireStar is a target and an input when it is the initiator.

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
PLOCK#	AE15	I/O (PCI)		**PCI Lock:** PLOCK# is used to indicate an atomic operation that may require multiple transactions to complete. When PLOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked. Control of PLOCK# is obtained under its own protocol in conjunction with PGNT#.
SERR#	AD17	I/O (PCI)		**System Error:** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, FireStar generates a non-maskable interrupt (NMI) to the 3.3V Pentium CPU.
PERR#	AE17	I/O (4mA)		**Party Error:** PERR# may be pulsed by any agent that detects a parity error during an address phase, or by the master or by the selected target during any data phase in which the AD[31:0] lines are inputs. Upon sampling PERR# active, FireStar generates a non-maskable interrupt (NMI) to the 3.3V Pentium CPU.
PCICLKIN	AB6	I		**PCI Clock Input:** Master PCI clock input on the CPU power plane. PCICLKIN is a 5.0V tolerant input, even when its power plane is connected to 3.3V as long as the 5VREF pins of FireStar are connected to +5.0V.
PIO6	AF16	I/O (PCI)	PCIDV1 86h ≠ 00h	**Programmable Input/Output 6:** See Section 3.3, "Programmable I/O Pins"
REQ0#	AF17	I		**PCI Bus Request 0:** REQ# is used by PCI bus masters to request control of the bus.
GNT0#	AD16	O (PCI)		**PCI Bus Grant 0:** GNT# is returned to PCI bus masters asserting REQ#, when the bus becomes available.
PIO7	AB18	I/O (4mA)	PCIDV1 87h ≠ 00h	**Programmable Input/Output 7:** See Section 3.3, "Programmable I/O Pins", on page 33 for more details.
PCICLK0	AB14 Strap option pin, refer to Table 3-7	O (PCI)		**PCI Clock Output 0:** This PCI clock output is always available.
PCICLK1	AB17	O (4mA)	RTCRD# strap option	**PCI Clock Output 1**
REQ2#	AB16	I	PCIDV1 88h = 00h	**PCI Bus Request 2:** REQ# is used by PCI bus masters to request control of the bus.
GNT2#	AB15	O (PCI)	Default	**PCI Bus Grant 2:** GNT# is returned to PCI bus masters asserting REQ#, when the bus becomes available.
REQ3#	AD18	I		**PCI Bus Request 3:** REQ# is used by PCI bus masters to request control of the bus.
GNT3#	AC18	O (PCI)		**PCI Bus Grant 3:** GNT# is returned to PCI bus masters asserting REQ#, when the bus becomes available.

8-3-3. IDE Interface Signal Set

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
Bus Master IDE Interface				
DBEW#	H24 Strap option pin, refer to Table 3-7	O (4mA)	Default	**Drive W Buffer Control**
DDRQ0	H25	I/O (4mA)	PCIDV1 89h=00h	**Drive Cable A DMA Request**
Clock and Reset Interface				
RESET#	AC24	O (8mA)		**System Reset:** When asserted, this signal resets the CPU. RESET# is asserted in response to a PWRGD only and is guaranteed to be active for 1ms such that CLK and VCC are stable. If RSTDRV is programmed to toggle in Suspend (via SYSCFG 40h[0]), so will RESET# since RESET# is derived from RSTDRV.
PWRGD	H26	I		**Power Good:** This input reflects the "wired-OR" status of the external reset switch and the power good status from the power supply.

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
OSC_14MHZ	E5	I		**Timer Oscillator Clock:** This is the main clock used by the internal 8254 timers. It is connected to a 14.31818MHz oscillator. OSC_14MHz is a 5.0V tolerant input, even when its power plane is connected to 3.3.V as long as the 5VREF pins of FireStar are connected to +5.0V.
OSC32	C7	I		**32KHz Clock:** This signal is used as a 32KHz clock input. It is used for power management and is usually the only active clock when the system is in Suspend mode. OSC32 is a 5.0V tolerant input, even when its power plane is connected to 3.3.V as long as the 5VREF pins of FireStar are connected to +5.0V.
CPUCLKIN	M5	I		**Feedback input to Circuitry:** This input clock must be equivalent to, and in phase with, the clock going to the CPU. **Note:** This is a CMOS-level input and therefore it is imperative that the rise time on this signal is less than or equal to 2.5ns.

8-3-4. ISA Interface Signal Set

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
Interrupt Controller Interface				
IRQ1	AF18	I	PCIDV1 8Ah = 00h	**Interrupt Request 1:** Normally connected to the keyboard controller. IRQ1 is a 5.0V tolerant input, even when its power plane is connected to 3.3.V as long as the 5VREF pins of FireStar are connected to +5.0V.
IRQA/IRQ3	AC19	I		**Programmable Interrupt Request A/IRQ3:** This input defaults to IRQ3, however, it can be programmed to route onto any ISA or PCI interrupt through PCIDV1 B0h. IRQA/IRQ3 is a 5.0V tolerant input, even when its power plane is connected to 3.3.V as long as the 5VREF pins of FireStar are connected to +5.0V.
IRQB/IRQ4	AD19	I		**Programmable Interrupt Request B/IRQ4:** This input defaults to IRQ4, however, it can be programmed to route onto any ISA or PCI interrupt through PCIDV1 B1h. IRQB/ITQ4 is a 5.0V tolerant input, even when its power plane is connected to 3.3.V as long as the 5VREF pins of FireStar are connected to +5.0V.
IRQC/IRQ5	AE19	I		**Programmable Interrupt Request C/IRQ5:** This input defaults to IRQ5, however, it can be programmed to route onto any ISA or PCI interrupt through PCIDV1 B2h. IRQC/IRQ5 is a 5.0V tolerant input, even when its power plane is connected to 3.3.V as long as the 5VREF pins of FireStar are connected to +5.0V.
IRQD/IRQ6	AF19	I		**Programmable Interrupt Request D/IRQ6:** This input defaults to IRQ6, however, it can be programmed to route onto any ISA or PCI interrupt through PCIDV1 B3h. IRQD/IRQ6 is a 5.0V tolerant input, even when its power plane is connected to 3.3.V as long as the 5VREF pins of FireStar are connected to +5.0V.
IRQC/IRQ7	AD20	I		**Programmable Interrupt Request E/IRQ7:** This input defaults to IRQ7, however, it can be programmed to route onto any ISA or PCI interrupt through PCIDV1 B4h.
IRQ8#	AE20	I	PCIDV1 8Bh = 00h	**Interrupt Request 8:** Normally connected to the RTC alarm output.
IRQF/IRQ9	AF20	I		**Programmable Interrupt Request F/IRQ9:** This input defaults to IRQ9, however, it can be programmed to route onto any ISA or PCI interrupt through PCIDV1 B5h.
IRQG/IRQ10	AB22	I		**Programmable Interrupt Request G/IRQ10:** This input defaults to IRQ10, however, it can be programmed to route onto any ISA or PCI interrupt through PCIDV1 B6h.
IRQH/IRQ11	AC21	I		**Programmable Interrupt Request H/IRQ11:** This input defaults to IRQ11, however, it can be programmed to route onto any ISA or PCI interrupt through PCIDV1 B7h.
IRQ12	AD21	I	PCIDV1 8Ch = 00h	**Interrupt Request 12:** Normally connected to the mouse interrupt from the keyboard controller.

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
IRQ14	AE21	I	PCIDV1 8Dh = 00h	**Interrupt Request 14:** Normally connected to the primary IDE channel.
IRQ15	AF21	I	PCIDV1 BBh[0] = 0	**Interrupt Request 15:** Normally connected to the secondary IDE channel.
IRQSER	AE18	I/O	PCIDV1 BAh[0] = 0	**Serial interrupt Request:** Bidirectional interrupt line for Compaq style of serial IRQs.
ISA DMA Arbiter Interface				
DRQA/DRQ0	M24	I	PCIDV1 99h = 00h	**Programmable DMA Request A/DRQ0:** The DRQ is used to request DMA service from the DMA controller. This input defaults to DRQ0, however, it can be programmed to route onto any internal DRQ by programming PCIDV1 C0h[2:0].
DRQB/DRQ1	M25	I	PCIDV1 9Ah = 00h	**Programmable DMA Request B/DRQ1:** The DRQ is used to request DMA service from the DMA controller. This input defaults to DRQ1, however, it can be programmed to route onto any internal DRQ by programming PCIDV1 C0h[6:4].
DRQC/DRQ2	M26	I	PCIDV1 9Bh = 00h	**Programmable DMA Request C/DRQ2:** The DRQ is used to request DMA service from the DMA controller. This input defaults to DRQ0, however, it can be programmed to route onto any internal DRQ by programming PCIDV1 C1h[2:0].
DRQD/DRQ3	L23	I	PCIDV 9Ch = 00h	**Programmable DMA Request D/DRQ3:** The DRQ is used to request DMA service from the DMA controller. This input defaults to DRQ3, however, it can be programmed to route onto any internal DRQ by programming PCIDV1 C1h[6:4].
DRQE/DRQ5	L24	I	PCIDV1 9Dh = 00h	**Programmable DMA Request E/DRQ5:** The DRQ is used to request DMA service from the DMA controller. This input defaults to DRQ5, however, it can be programmed to route onto any internal DRQ by programming PCIDV1 C2h[6:4].
DRQF/DRQ6	M25	I	PCIDV1 9Eh = 00h	**Programmable DMA Request F/DRQ6:** The DRQ is used to request DMA service from the DMA controller. This input defaults to DRQ6, however, it can be programmed to route onto any internal DRQ by programming PCIDV1 C3h[2:0].
DRQG/DRQ7	L26	I	PCIDV1 9Fh = 00h	**Programmable DMA Request G/DRQ6:** The DRQ is used to request DMA service from the DMA controller. This input defaults to DRQ7, however, it can be programmed to route onto any internal DRQ by programming PCIDV1 C3h[6:4].
DACKA#/DACK0#	K22	O		**Programmable DMA Acknowledge A/DACK0#:** DACK# is used to acknowledge DRQ to allow DMA transfer. This input defaults to DACK0#, however, it can be programmed to route onto any internal DACK# by programming PCIDV1 C0h[2:0].
PPWR4			PCIDV1 C0h[2:0] = 100	**Peripheral power control Line 4:** Peripheral power control lines 0 through 15 are latch outputs used to control external devices.
DACKB#/DACK1#	K23	O		**Programmable DMA Acknowledge B/DACK1#:** DACK# is used to acknowledge DRQ to allow DMA transfer. This input defaults to DACK1#, however, it can be programmed to route onto any internal DACK# by programming PCIDV1 C0h[6:4].
DACKC#/DACK2#	K24	O		**Programmable DMA Acknowledge C/DACK2#:** DACK# is used to acknowledge DRQ to allow DMA transfer. This input defaults to DACK2#, however, it can be programmed to route onto any internal DACK# by programming PCIDV1 C1h[2:0].
DACKD#/DACK3#	K25	O		**Programmable DMA Acknowledge D/DACK3#:** DACK# is used to acknowledge DRQ to allow DMA transfer. This input defaults to DACK3#, however, it can be programmed to route onto any internal DACK# by programming PCIDV1 C1h[6:4].
DACKE#/DACK5#	K26	O		**Programmable DMA Acknowledge E/DACK5#:** DACK# is used to acknowledge DRQ to allow DMA transfer. This input defaults to DACK5#, however, it can be programmed to route onto any internal DACK# by programming PCIDV1 C2h[6:4].
DACKE#/DACK6#	J22	O		**Programmable DMA Acknowledge F/DACK6#:** DACK# is used to acknowledge DRQ to allow DMA transfer. This input defaults to DACK6#, however, it can be programmed to route onto any internal DACK# by programming PCIDV1 C3h[2:0].
DACKG#/DACK7#	J23	O		**Programmable DMA Acknowledge G/DACK7#:** DACK# is used to acknowledge DRQ to allow DMA transfer. This input defaults to DACK7#, however, it can be programmed to route onto any internal DACK# by programming PCIDV1 C3h[6:4].

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
Compact ISA Interface				
PIO15	AC25	I/O (4mA)	PCIDV1 8Fh ≠ 00h	**Programmable Input/Output 15:** See Section 3.3, "Programmable I/O Pins", on page 33 for more details.
SD[15:0]	Refer to Table 3-2	I/O (8nA)	Cycle Multiplexed	**System Data Bus:** SD[15:0] provides the 16-bit data path for devices residing on the ISA bus.
MAD[15:0]				**Multiplexed Address/Data Bus:** Used during CISA cycles.
PIO14	AC20	I/O (4mA)	PCIDV1 8Eh ≠ 00h	**Programmable Input/Output 14:** See Section 3.3, "Programmable I/O Pins", on page 33 for more details.
CMD#	AB20	O (4mA)	SYSCFG 16h[7, 5]	**Command:** Dedicated CISA output used to signal a data transfer command.
DIRTY		I/O (4mA)		**Tag Dirty Bit:** This dirty bit allows the tag data to be 8 bit wide instead of 7.
ATCLK	AA22	O (8mA)		**ISA Bus Clock:** This signal is derived from an internal division of PCICLK. It is used to sample and drive all ISA synchronous signals. PCIDV1 47h[5:4] sets the ATCLK: 00 = PCICLK+4 10 = PCICLK+2 01 = PCICLK+3 11 = PCICLK The ATCLK is also used to demultiplex and sample externally multiplexed inputs. During Suspend, it is possible to output 32KHz on this pin, or drive it low.
IOCHRDY	AB26	I/O (8mA)		**I/O Channel Ready:** Resources on the ISA bus deassert IOCHRDY to indicate that wait states are required IOCHRDY to indicate that wait states are required to complete the cycle. IOCHRDY is an input when FireStar owns the ISA bus and is an output when an external ISA bus master owns the ISA bus. IOCHRDY is automatically tristated in Suspend.
BALE	W22	O (8mA)		**Bus Address Latch Enable:** BALE is an active high signal asserted to indicate that the address, AEN, and SBHE# signal lines are valid. BALE remains asserted throughout ISA master and DMA cycles.
ISA Bus Interface				
MRD#	AC26	I/O (8mA)		**Memory Read:** MRD# is the command to a memory slave that it may drive data onto the ISA data bus. MRD# is an output when FireStar is a master on the ISA bus. MRD# is an input when an ISA master, other than FireStar, owns the ISA bus.
MWR#	AB23	I/O (8mA)		**Memory Write:** MWR# is the command to a memory slave that it may latch data from the ISA data bus. MWR# is an output when the FireStar owns the ISA bus. MWR# is an input when an ISA master, other than FireStar, owns the ISA bus.
IOR#	AB24	I/O (8mA)		**I/O Read:** IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus (SD[15:0]). The I/O slave device must hold the data valid until after IOR# is negated. IOR# is an output when FireStar owns the ISA bus. ISA# is an input when an external ISA master owns the ISA bus.
IOW#	AB25	I/O (8mA)		**I/O Write:** IOW# is the command to an ISA I/O slave device that the slave may drive latch data from the ISA data bus (SD[15:0]). IOR# is an output when FireStar owns the ISA bus. IOW# is an input when an external ISA master owns the ISA bus.
SMRD#	W26	I/O (8mA)	PCIDV1 95h = 00h	**System Memory Read:** FireStar asserts SMRD# to request a memory slave to provide data. If the access is below the 1MB range (00000000h-000FFFFFh) during DMA compatible, IPC master, or ISA master cycles, FireStar asserts SMRD.
SMWR#	V22	I/O (8mA)	PCIDV1 96h = 00h	**System Memory Write:** FireStar asserts SMWR# to request a memory slave to accept data from the data lines. If the access is below the 1MB range (00000000h-000FFFFFh) during DMA compatible, IPC master, or ISA master cycles, FireStar asserts SMWR#.
AEN	M22	I/O	PCIDV1 C2h [1] = 0	**Address Enable:** AEN is asserted during DMA cycles to prevent I/O slaves from misinterpreting DMA cycles as valid I/O cycles. When asserted, AEN indicates to an I/O resource on the ISA bus that a DMA transfer is occurring. This signal is asserted also during refresh cycles. AEN is driven low upon reset.
IO16#	W23	I/O	PCIDV1 92h = 00h	**16-Bit I/O Chip Select:** This signal is driven by I/O devices on the ISA bus to indicate that they support 16-bit I/O bus cycles.

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
M16#	W24	I/O	PCIDV1 93h = 00h	**16-Bit Memory Chip Select:** ISA slaves that are 16-bit memory devices drive this signal low. MEMCS16# is an input when FireStar owns the ISA bus. FireStar drives this signal low during ISA master to PCI memory cycles.
RFSH#	J25	I/O	PCIDV1 C2h[0] = 0	**Refresh:** As an output, this signal is used to inform FireStar to refresh the local DRAM. During normal operation, a low pulse is generated every 15µs to indicate to FireStar that the DRAM is to be refreshed if PCIDV1 64h[0] = 0. During Suspend, if normal DRAM is used, the 32KHZ input to the FireStar is routed out on this pin so that it may perform DRAM refresh. An option to continuously drive this signal low during Suspend is also provided. The internal pull-up on this pin is disengaged in Suspend.
SBHE#	W25	I/O	PCDIDV1 94h = 00h	**System Byte High Enable:** When asserted, SBHE# indicates that a byte is being transferred on the upper byte (SD[15:8]) of the data bus. SBHE# is negated during refresh cycles. SBHE# is an output when FireStar owns the ISA bus.
TC	M23	I/O	PCIDV1 C2h [2] = 0	**Terminal Count**
XD7	AA23	I/O (8mA)	Cycle Multiplexed (See Note)	**XD Bus Line 7:** ISA status signal.
IDE_DCS3#				**DCS3 Control for Primary IDE Channel**
XD6	AA24	I/O (8mA)	Cycle Multiplexed (See Note)	**XD Bus Line 6:** ISA status signal.
IDE_DCS1#				**DCS1 Control for Primary IDE Channel**
XD5	AA25	I/O (8mA)	Cycle Multiplexed (See Note)	**XD Bus Line 5:** ISA status signal.
IDE_DDACK#				**DMA Acknowledge for Primary IDE Channel**
XD4	AA26	I/O (8mA)	Cycle Multiplexed (See Note)	**XD Bus Line 4:** ISA status signal.
IDE_DA2				**Address Bit 2 for Primary IDE Channel**
XD3	Y23	I/O (8mA)	Cycle Multiplexed (See Note)	**XD Bus Line 3:** ISA status signal.
IDE_DA1				**Address Bit 1 for Primary IDE Channel**
XD2	Y24	I/O (8mA)	Cycle Multiplexed (See Note)	**XD Bus Line 2:** ISA status signal.
IDE_DA0				**Address Bit 0 for Primary IDE Channel**
XD1	Y25	I/O (8mA)	Cycle Multiplexed (See Note)	**XD Bus Line 1:** ISA status signal.
IDE_DRD#				**Drive Read Control for Primary IDE Channel**
XD0	Y26	I/O (8mA)	Cycle Multiplexed (See Note)	**XD Bus Line 0:** ISA status signal.
IDE_DWR#				**Drive Write Control for Primary IDE Channel**
Note: XD[7:0] can be strapped to be dedicated IDE lines via the RTCAS:A20M# strap option and PCIDV1 75h[6] = 1				
SA[23:20]	V23:V26	I/O (8mA)		**System Address Bus Lines 23 through 20:** The SA[23:0] signals on FireStar provide the address for memory and I/O accesses on the ISA bus. The address are outputs when FireStar owns the ISA bus and are inputs when an external ISA master owns the ISA bus.
SA[19:18]	U23:U24	I/O (8mA)		**System Address Bus Lines 19 and 18**
SA[17:16]	U25:U26	I/O (8mA)	PCIDV1 91h-90h = 00h	**System Address Bus Lines 17 and 16**
SA[15:0]		I/O (8mA)		**System Address Bus Lines 15 through 0**
External Real-Time Clock Interface				
RTCAS	N24	O (4mA)		**Real-Time Clock Address Strobe:** This signal is connected to the address strobe of the real-time clock.
RTCRD#	N25	O (4mA)		**Real-Time Clock Read:** This pin is used to drive the read signal of the real-time clock.
RTCWR#	N26	O (4mA)		**Real-Time Clock Write:** This pin is used to drive the write signal of the real-time clock.
Power Management Unit Interface				
PPWR0#	AC23	I/O	BOFF# strap option	**Peripheral Power Control Line 0#**

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
Miscellaneous				
A20M#	R3	O (4mA)		**Address Bit 20 Mask:** This pin is an output and generates the A20M# output by trapping GATEA20 commands to the keyboard or to Port 092h. The CPUINIT signal to the CPU is generated whenever it senses reset commands to Port 060h/064h, or a Port 092h write command with bit 0 set high. When keyboard emulation is disabled, FireStar traps only Port 092h GATEA20 commands and accepts the GATEA20 input from the keyboard controller, which os sent out as A20M# to the CPU.
ROMCS#	J24	O (4mA)	PCIDV1 52h[2] = 0 97h = 00h 4Fh[1] = 0	**BIOS ROM Chip Select:** This output goes active on both reads and writes to the ROM area to support flash ROM. For flash ROM support, writes to ROM can be supported by appropriately setting PCIDV1 47h[7].
SPKROUT	H23	I/O (8mA)		**Speaker Data:** This pin is used to drive the system board speaker. This signal is a function of the Timer-0 Counter-2 and Port 061h bit 1. Can use CISA Protocol to gang several.
KBDCS#	J26	O (8mA)	Default PCIDV1 98h = 00h	**Keyboard Chip Select:** Used to decode accesses to the keyboard controller.

8-3-5 Test Mode Selection Pins

Signal Name	Pin No.	Signal Type (Drive)	Selected By	Signal Description
RSVD	B7 Strap option pin for future 2.5V CPU interface, refer to Table 3-7	I/O (4mA)		**Reserved:** This pin is reserved for possible additional functionality on future revisions of FireStar. However, it is used as an input for the ATE Test Mode selection address. See TMS (pin AB5) description.
RSVD	A7	I/O (4mA)		**Reserved in FireStar:** An input for the ATE Test Mode selection address. See TMS (Pin AB5) description.
TMS	AB5	I/O		**Test Mode Select:** An input for the ATE Test Mode selection address. AB5 B7 A7 Mode 0 X X Normal operation (default) 1 0 0 Tristate all pins 1 0 1 NAND tree test 1 1 0 Reserved for factory test 1 1 1 Reserved for Factory test

8-3-6 Power and Ground Pins

Signal Name	Pin No.	Signal Type	Signal Description
GND	AA6, AA13, AA14, AA21, AB13, E14, F6, F13, F14, F21, N5, N6, N21, P6, P21, P22	G	**Ground Connections**
VCC_ISA	L22, U22, Y22	P	**ISA Bus Power Plane: 3.3V or 5.0V**
VCC_CPU	E8, G5, T5, W5	P	**CPU Bus Power Plane: 3.3V (and 2.5V in future 2.5V CPU interface revision)**
VCC_CORE	AB19, H22, K5,	P	**FireStar Core power Plane: 3.3V only**
VCC_DRAM	E11, E17, E20	P	**Memory Power Plane: 3.3V or 5.0V**
VCC_PCI	AB7, AB10, AB16	P	**PCI Bus Power Plane: 3.3V or 5.0V**
5VREF	AB21, E7	P	**5.0V Reference:** Connect to 5.0V is available in the system. Connect to 3.3V for an all 3.3V design.

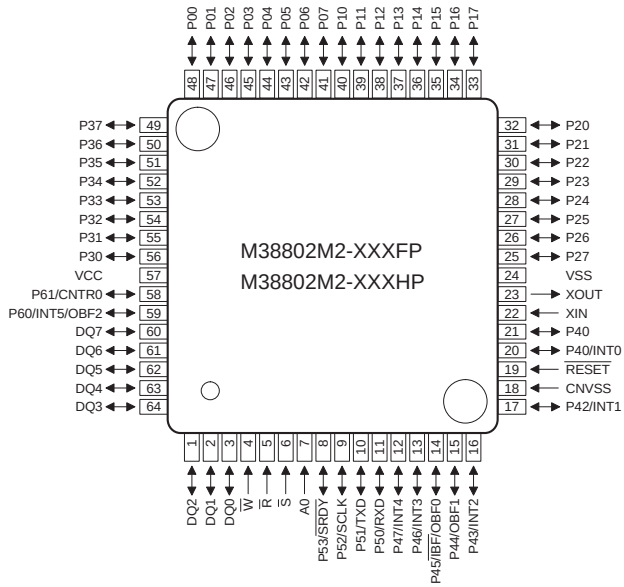
9. PS/2 Keyboard Controller

9-1. Introduction

The keyboard and mouse are controlled using Mitsubishi Electric's M38802M270.

No PS/2 type mouse can be used for UP-5300 because IRQ12 is not connected. In addition, A20M# of M38802M2 is not used because Firestar's A20M# is used.

9-2. Pin assignments

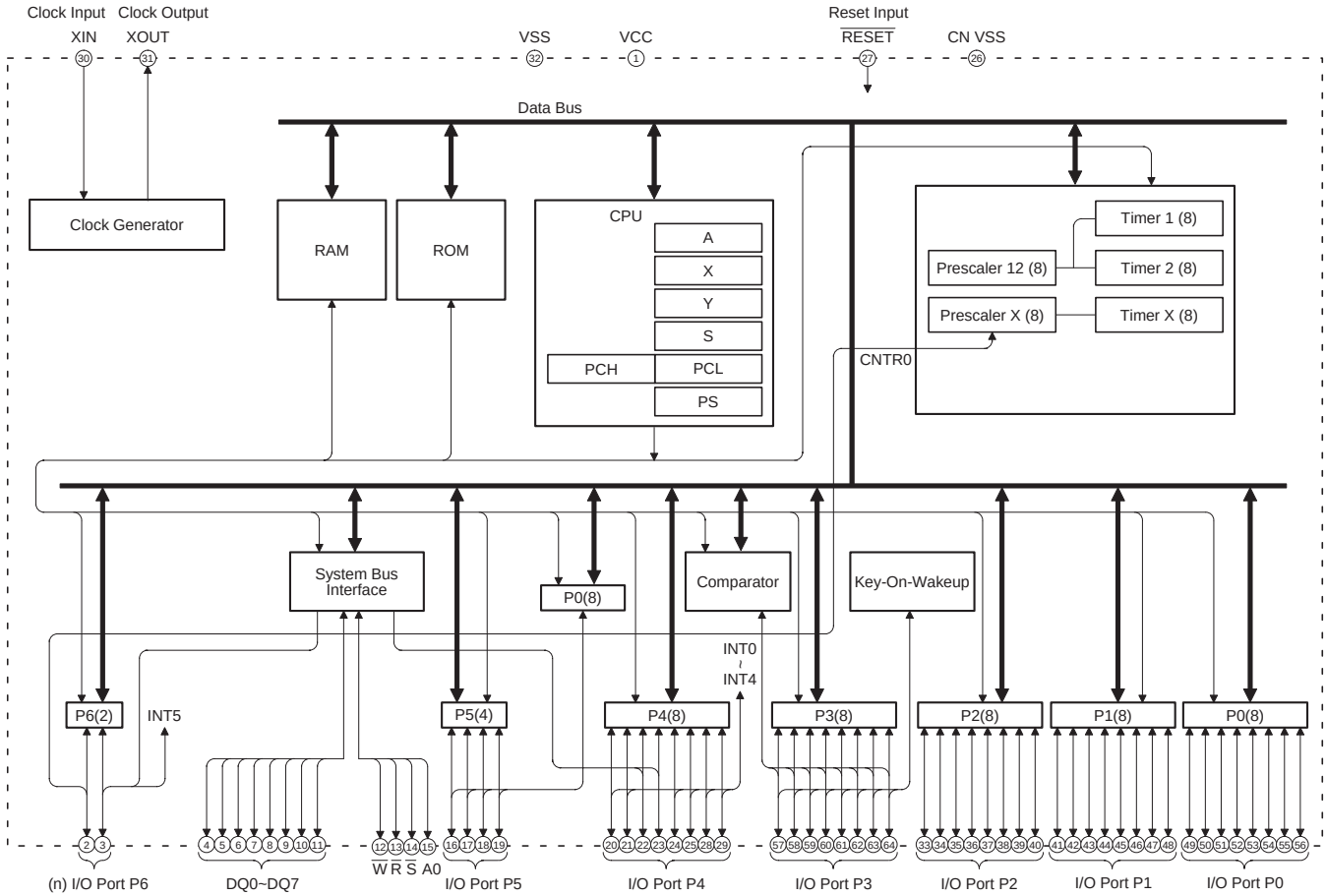


9-3. Pin description

Pin	Name	Features	Features other than port
Vcc, Vss	Power input	Impresses Vcc with 2.7 to 5.5V, and Vss with 0V.	
CNVss	CNVss	Pin controlling the operation mode of chip. Connect this pin to Vss.	
RESET	Reset input	Pin for the reset input of active "L".	
XIN	Clock input	Pin for the I/O of clock generator. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. When using external clock, connect a clock generator to XIN and open XOUT. A feedback resistor is incorporated.	
XOUT	Clock output		
P00 ~ P07	I/O port P0	8-bit I/O port. I/O can be specified in bits using a program. When resetting, these ports go into input mode. CMOS input level is used, and the form of output is CMOS 3-state.	
P10 ~ P17	I/O port P1		
P20 ~ P27	I/O port P2	8-bit I/O port with the same feature as P0. CMOS input level is used, and the form of output is CMOS 3-state. The 4 bits of P24 to P27 can output large current for driving LED's.	
P30 ~ P37	I/O port P3	8-bit I/O port with the same feature as P0. CMOS input level is used, and the form of output is CMOS 3-state. Whether to use any internal pull up resister or not can be selected using a program.	Key input (key on wakeup interrupt input) pin Comparator input pin
P40	I/O port P4	8 bits I/O port with almost the same feature as P0. Input level can be switched between CMOS and TTL, and the form of output can be switched between CMOS 3-state and N-channel open drain. Pin level can be inputted regardless of the setting of input port or output port.	
P41/INT0, P42/INT1, P43/INT2			Interrupt input pin
P44/OBF0, P45/IBF/ OBF1			Data bus buffering pin
P46/INT3, P47/INT4			Interrupt input pin
P50/RxD, P51/TxD, P52/SCLK, P53/SRDY	I/O port P5	4-bit I/O port with almost the same feature as P0. CMOS input level is used, and the form of output is CMOS 3-state.	Serial I/O pin
P60/INT5/ OBF2	I/O port P6	2-bit I/O port with almost the same feature as P0. CMOS input level is used, and the form of output is CMOS 3-state.	Interrupt input pin Data bus buffering pin
P61/CNTR0			Timer X pin

Pin	Name	Features	Features other than port
A0, S, E/R, R/W/W	Input port	Control bus for the host CPU. Input level can be switched between CMOS and TTL.	
DQ0 ~ DQ7	I/O port	8-bit data bus for the host CPU. Input level can be switched between CMOS and TTL.	

9-4. Functional block diagram



10. Video Subsystem

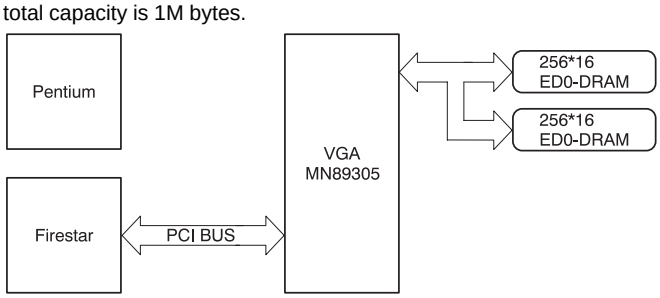
10-1. Introduction

UP-5300 adapts the VGA controller (MN89305) to allow the following type of LCD panel.

LM10V33 (640 × 480 XRGB DSTN 256 color)

The display data format of the MN89305 is 16 bpp. In the 16-bpp format Data in memory directly becomes R, G and B data, and makes it possible to select between the R(5)+G(6)+B(5) and R(5)+G(5)+B(5) formulation. For the area of less than 6bits, 5-bit data is positioned to the 5 higher-order bits. This data is output passing through the gray scale engine block and half frame control block to the LCD.

UP-5300 connects a PCI bus as the interface, and uses 2 chips of EDO DRAM configured in 256K × 16 as graphic memory so that the total capacity is 1M bytes.



Host Type Setting

Host Type	MA2	MA1	MA0	Selection
PCI	H	L	L	UP-5300 Setting

Setting H = 10kohm Pull up (Vcc3)

L = 10kohm Internal pull down

On the MN89305, it is possible to select up to three kinds of initialization parameters of the LCD panel on the VGA BIOS. When the panel described above is to be used, the following settings must be required.

Expansion terminal setting

Panel Type	MA5	MA4	MA3	Selection
LCD Color Dual Scan	(L)	(L)	(L)	UP-5300 Setting

Setting = 10kohm Pull up (Vcc3)

(L) = 100kohm Internal pull down

MA9-6: not used (100kohm Internal pull down)

10-2. Pin assignments

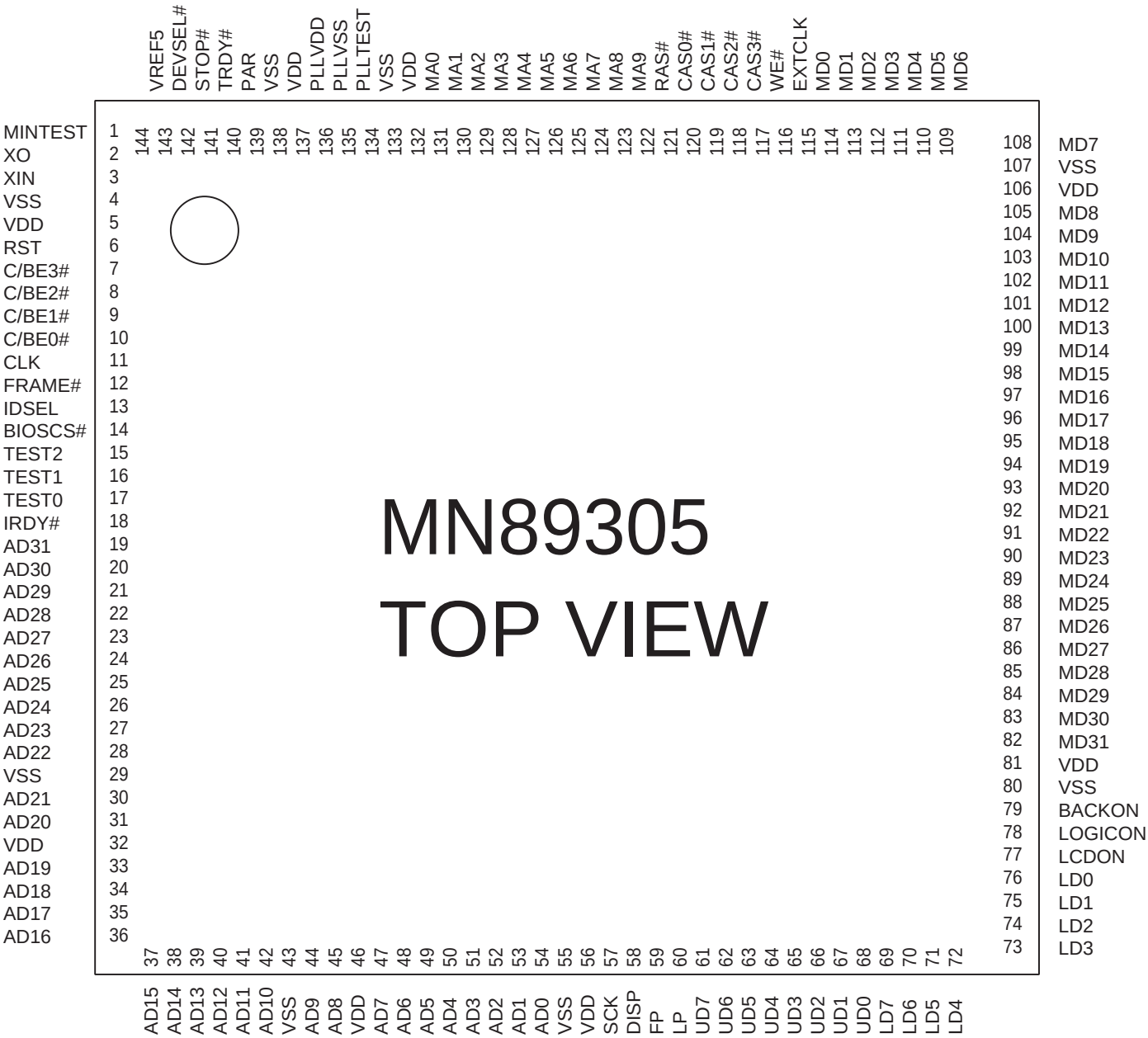


Figure 2-1: Pin Diagram

10-3. Pin description

10-3-1. PCI bus-related pins

Pin name	I/O	Level	Function
CLK	I	5VTTL	PCI Clock PCI bus synchronization clock. Possible to input up to 33MHz.
AD[31:0]	I/O	5VTTL	Address Data Bus Time shared PCI bus address or data bus
C/BE[3:0]#	I	5VTTL	Command/Byte Enable In the address phase, it represents memory access, I/O access, configuration access and read/write command. In the data phase, it functions as the byte enable signal.
PAR	I/O	5VTTL	Bus Parity Parity input, and parity output for the read command
FRAME#	I	5VTTL	Cycle Frame The period during which data is transferred. The transfer cycle starts when input is low and is terminated by the next transfer data of high input.
IRDY#	I	5VTTL	Initiator Ready One data phase ends in a cycle where both IRDY# and TRDY# are LOW simultaneously.
TRDY#	O		Target Ready One data phase ends in a cycle where both IRDY# and TRDY# are LOW simultaneously.
STOP#	O		Stop This signal is output when this LSI aborts the data transfer being currently executed.
IDSEL	I	5VTTL	Initialization Device Select The chip select signal of configuration register. The configuration register can be accessed when this signal is high. It is recommended to connect the AD24 to AD31 when the AD signal is used as IDSEL.
DEVSEL#	O		Device Select LOW is output when the request for accessing the LSI is detected.
BIOSCS#	O		BIOS Chip Select LOW is output when access to VIDEO BIOS is accepted.

10-3-2. Memory access-related pins

Pin name	I/O	Level	Function
MA[9:0]	I/O	CMOS	Memory Address Address for display memory It becomes input mode when resetting. MA[2:0] determines the host type of the chip. MA[9:3] is taken into the internal latch as data about the expansion terminal monitor register.
RAS#	O		RAS Address Strobe This output is the strobe signal for low address latch.
CASO#	O		Lower CAS Address Strobe for RAMO This output is the strobe signal for RAMO's lower byte column address.
CAS1#	O		Upper CAS Address Strobe for RAMO This output is the strobe signal for RAMO's upper byte column address.
CAS2#	O		Lower CAS Address Strobe for RAM1 This output is the strobe signal for RAM1's lower byte column address.
CAS3#	O		Lower CAS Address Strobe for RAM1 This output is the strobe signal for RAM1's upper byte column address.
WE#	O		Write Enable This output is the data write signal.
MD[31:0]	I/O	CMOS	Memory Data bus This is DRAM memory data. Can be switched to the 16-bit bus by changing the register setting. This data bus is also used for reading the video BIOS through PCI bus connection. MD[15:0] and MD[23:16] correspond to the BIOS ROM address and BIOS ROM data input, respectively.

10-3-3. LCD-related pins

Pin name	I/O	Level	Function
BACKON	I/O	CMOS	Back Light On This output is the signal which requests lighting of the back light. LOW: Off HIGH: On This terminal can also be used as a general-purpose I/O port. In the external RAMDAC mode, this terminal outputs the register WR signal to RAMDAC.

Pin name	I/O	Level	Function
LCDON	I/O	COMS	LCD Driving Power Supply On This output is the signal which requests turning-on of the power supply for driving the LCD panel on. LOW: Off HIGH: On This terminal can also be used as a general-purpose I/O port. In the external RAMDAC mode, this terminal outputs the register address Bit0 to RAMDAC.
LOGICON	I/O	CMOS	LCD Logic Power Supply On This output is the signal which requests turning on of the logic power supply for the LCD panel. LOW: Off HIGH: On This terminal can also be used as a general-purpose I/O port. In the external RAMDAC mode, this terminal outputs the register address Bit1 to RAMDAC.
LP	O		Latch Pulse This output is the pulse which indicates the 1-line data latch timing of the STNLCD panel. For the TFTLCD panel and in the external RAMDAC mode, it indicates a horizontal synchronizing signal.
FP	O		Frame Pulse This output is the pulse which indicates the frame start of the STNLCD panel. For the TFTLCD panel and in the external RAMDAC mode, it indicates a vertical. synchronizing signal.
DISP	O		Display Enable This output is the signal which enables the LCD to display. It is used as the blanking signal in the external RAMDAC mode and as the display enable signal for the TFTLCD panel.
SCK	O		Shift Clock This output is the data shift clock to the STNLCD panel. The dot clock is output for the TFTLCD panel and in the external RAMDAC mode.
UD[7:0] LD[7:0]	O		Upper/Lower Data 7:0 This is data for outputting display data. In the external RAMDAC mode, LD[7:0] is display data while UD[7:0] is write data line to the RAMDAC register

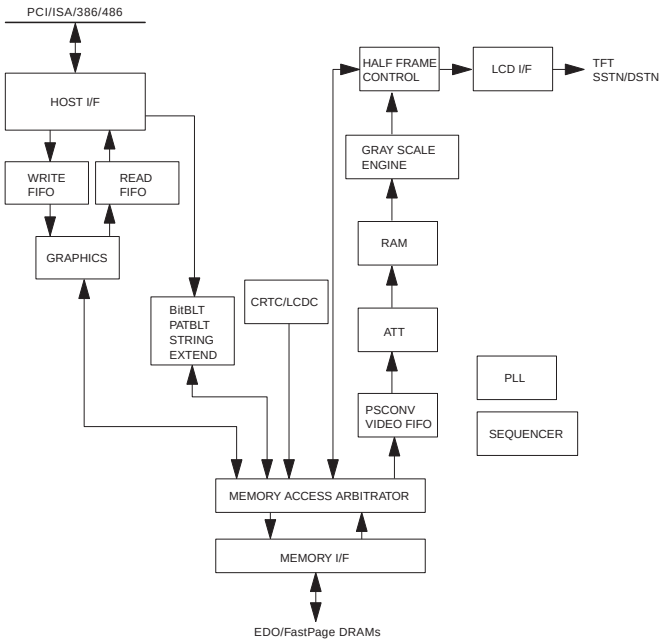
10-3-4. Chip settings

Pin name	I/O	Level	Function
RESET/RST	I	5VTTL	RESET(ISA)/RST(386, 486, PCI) The chip is reset to the initial state when this input is at high. This reset signal controls the phase of the clock when the host is in the 386 mode. Remember that this terminal is positive logic.
MA[2:0]	I	CMOS	HOST Type MA[2:0] remains in the input mode during setting. In the input mode, it is used as the terminal that sets the host type to be connected. Settings other than given below are prohibited. MA[2:0] Host Type 0 0 0 ISA 0 0 1 386SX 0 1 0 386DX 0 1 1 486 1 0 0 PCI
XIN/XO	I/O	CMOS	Clock In/Out This is the clock I/O of the chip. Connect a crystal resonator. This is used for the display clock. The refresh rate of the LCD panel is determined by the input frequency of this pin. The input frequency must be from 4MHZ to 30MHz.
EXTCLK	I	CMOS	EXTERNAL MCLK Input from this terminal is used as an MCLK instead of the oscillation of the built-in PLL. If the oscillation starts when the reset is active, the PLL automatically becomes disable and the signal from this terminal is used as the MCLK. Input the signal at a higher clock frequency than XIN and within the range from 35MHz to 65MHz. Secure it to VDD or VSS when not used.
MINTEST TEST[2:0]	I I	COMOS 5VTTL	TEST Secure the MINTEST pin to VSS. Secure to VSS for operation. (PCI mode only)
PLLTEST	I/O		Terminal for testing PLL. Secure to VSS for operation.

10-3-5. Power Supply

Pin name	I/O	Level	Function
VDD			Digital system power supply terminal (3.3V system)
VSS			Digital system power supply terminal (GND)
PLL VDD			PLL analog system power supply terminal (3.3 V system)
PLL VSS			PLL analog system power supply terminal (GND)
VREF5			Power supply terminal for 5V input terminal (4.75 V to 5.25 V)

10-4. Functional block diagram



11. Super I/O

11-1. Introduction

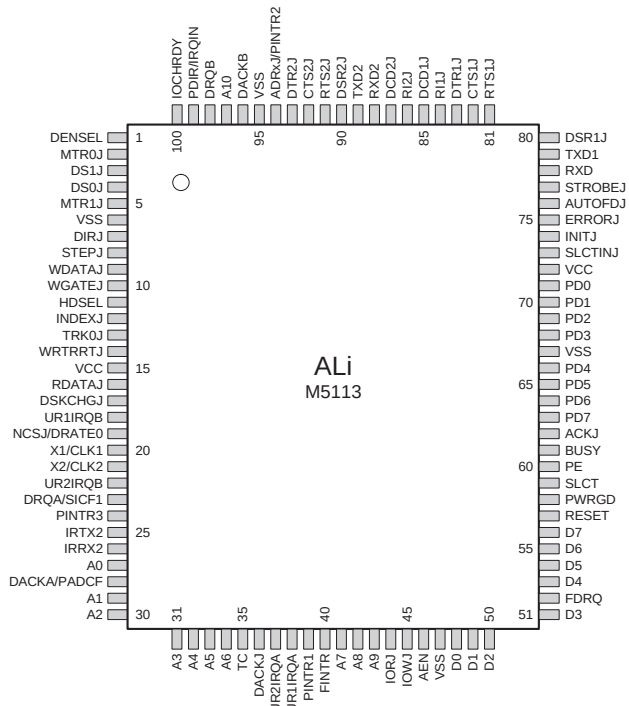
The FDC, serial port COM1 and COM2, and parallel port LPT1 are controlled by ALi's M5113A2.

M5113 Hardware Setting Configuration

Pin No.	Pin Name	Setting	Function
23	DRQA/S1CF1	1	UART1
24	PINTR3/S1 CF0	1	I/O address = 3F8h (COM1)
93	DTR2J/S2CF1	1	UART2
91	RTS2J/S2CF0	1	I/O address = 2F8h (COM2)
81	RTS1J/PFF1	1	LPT
79	TXD1/PCF0	0	I/O address = 378h (LPT1)
94	DRV2/ADRxJ/ PINTR2/ECPEN1	0	Parallel Port Mode Enhanced Parallel Port
83	DTR1J/ECPEN0	1	
89	TXD2/FDCCF	0	Floppy disk state
26	IRRX2/FACF	1	FDC disable, config port 398h
25	IRTX2/CFG2	1	Configuration port 398h (Internal pull up)

Setting 1 = Pull up (Vcc5)
0 = Pull down

11-2. Pin assignments



11-3. Pin description

A low represents a logic 0 (0V nominal) and a high represents a logic 1 (+2.4V nominal).

Name	Number	Type	Description
HOST Processor Interface			
D0-D7	48-51, 53-56	I/O24	**Data bus.** This connection is used by the host microprocessor to transmit data to and from the M5113. These pins are in a high impedance state when not in the output mode.
IORJ	44	I	**I/O Read.** This active low signal is issued by the host microprocessor to indicate a read operation.
IOWJ	45	I	**I/O Write.** This active low signal is issued by the host microprocessor to indicate a write operation.
AEN	46	I	**Address Enable.** This active high signal indicates DMA operations on the host data bus.
A0-A9	27, 29-34, 41-43	I	**I/O Address.** These bits determine the I/O address to be accessed during IORJ and IOWJ cycles.
DACKA/ PADCF	28	I	**DMA Acknowledge.** An active low input signal acknowledging the request for a DMA transfer of data between the host and the printer port. This input enables the DMA read or write internally. This active high signal is read and latched during reset active.
FDRQ	52	O24	**FDC DMA request.** This active high output is the DMA request for byte transfers of data to the host. This signal is cleared on the last byte of the data transfer by the DACKJ signal going low (or by IORJ going low if DACKJ was already low as in demand mode).
DACKJ	36	I	**DMA acknowledge.** This active low input acknowledging the request for a DMA transfer of data. This input enables the DMA read or write internally.
TC	35	I	**Terminal Count.** This signal indicates to the M5113 that data transfer is complete. TC is only accepted when DACKJ or PDACKJ is low. In AT, TC is active high and in PS/2 mode, TC is active low.
UR1IRQA	38	O24	**Primary Serial Port Interrupt.** UR1IRQA is a source of PSP interrupt. Externally, it should be connected to IRQ4 on PC/AT.
UR2IRQA	37	O24	**Secondary Serial Port Interrupt.** UR2IRQA is a source of SSP interrupt. Externally, it should be connected to IRQ3 on PC/AT.
FINTR	40	O24	**FDC Interrupt Request.** This interrupt from the Floppy Disk Controller is enabled/disabled via bit 3 of the Digital Output Register (DOR).
PINTR1	39	O24	**Parallel Port Interrupt Request.** This request from the Parallel Port is enabled/disabled via bit 4 of the Parallel Port Control Register. If EPP or ECP mode is enabled, this output is pulsed low, then released to allow sharing of interrupts.
RESET	57	IS	**Reset.** This active high signal resets the M5113 and must be valid for 500 ns minimum. In M5113, the falling edge of reset latches the jumper configuration. The jumper select lines must be valid 50 ns prior this edge.
Floppy Disk Interface			
RDATAJ	16	IS	**Read Disk Data.** The active-low, raw data read from the disk is connected here. Each falling edge represents a flux transition of the encoded data.
WGATEJ	10	O36	**Write Gate.** This active-low, high-drive output enables the write circuity of the selected disk drive. This signal prevents glitches during power-up and power-down. This signal prevents writing to the disk when power is cycled.
WDATAJ	9	O36	**Write Data.** This active low output is a write-precompensated serial data to be written onto the selected disk drive. Each falling edge causes a flux change on the media.
HDSELJ	11	O36	**Head Select.** This active low output determines which disk drive head is active. Low = Head 0, high (open) = Head 1.
DIRJ	7	O36	**Direction.** This active low output determines the direction of the head movement (low = step-in, high = step-out). During the write of read modes, this output is high.
STEPJ	8	O36	**Step.** This active low output produces a pulse at a software-programmable rate to move the head during a seek operation.
DSKCHGJ	17	IS	**Disk Change.** This disk interface input indicates when the disk drive door has been opened. This active-low signal is read from bit D7 of address xx7h.
DS0J, DS1J	4, 3	O36	**Drive Select 0,1.** Active low, output signal selects drives 0-1.
IRQIN/ PDIR	99	I O4	This pin is a multi-function pin. This pin can be used as IRQIN to steer an interrupt signal from external device onto either UR1IRQB (Pin 18) or UR21RQB (Pin 22). This pin is PDIR when used to indicate the direction of the Parallel port data bus. 0 = output/write, 1 = input/read.
A10	97	I	This pin is the A10 address input.
MTR0J, MTR1J	2, 5	O36	**Motor on 0, 1.** These active-low output select motor drives 0-1.
DACKB	96	I	This signal is the Parallel port DMA acknowledge input.
DRQB	98	O24	In ECP mode, this is the Parallel Port DMA Request output active high signal.
DENSEL	1	O36	**Density select.** This signal indicates whether a low (250/300 kbps) or high (500 kbps) data rate has been selected. This is determined by the DENSEL bits in Configuration register 5.

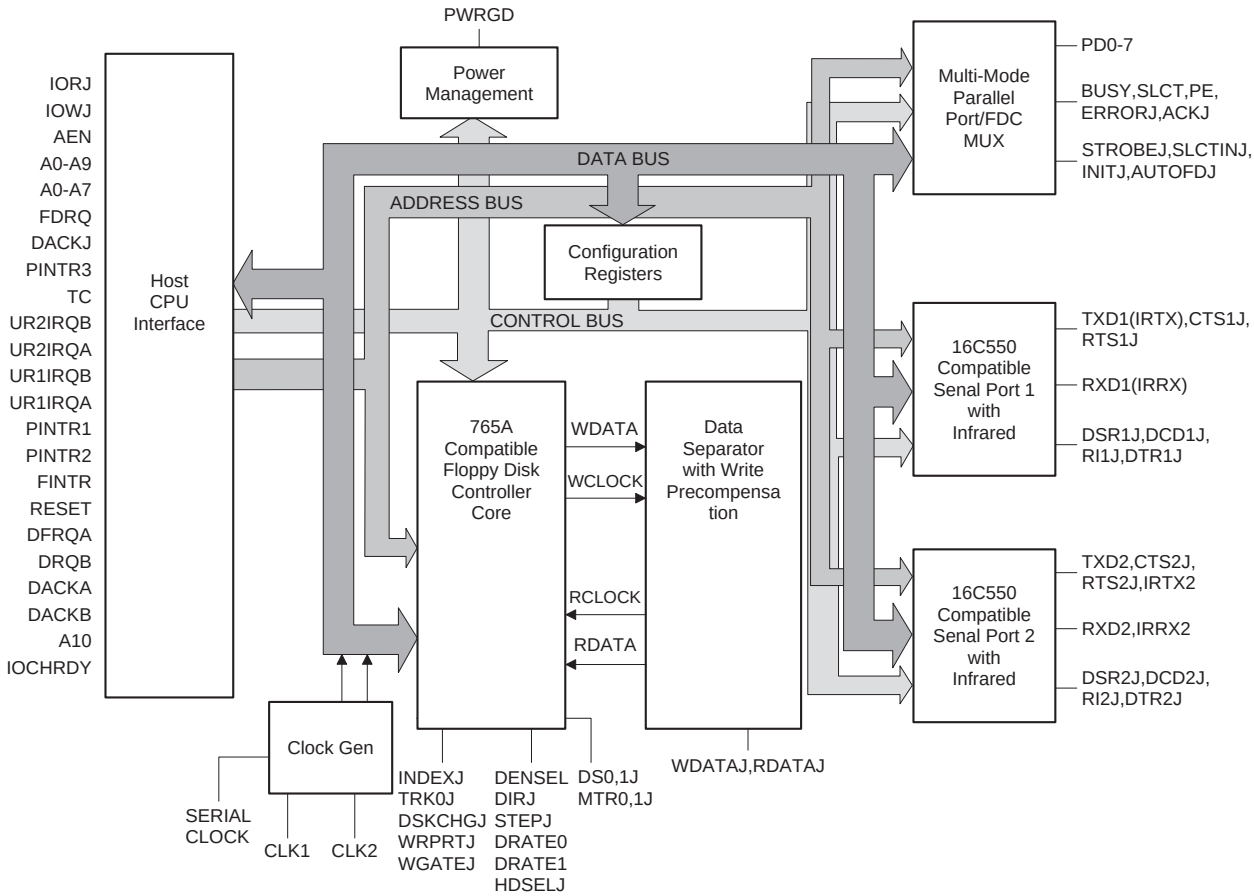
Name	Number	Type	Description
WRTPRTJ	14	IS	**Write Protected.** This active-low Schmitt Trigger input senses from the disk drive that a disk is write-protected. Any write command is ignored.
TRK0J	13	IS	**Track 00.** This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the outermost track.
INDEXJ	12	IS	**Index.** This active low Schmitt Trigger input senses form the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
UR1IRQB	18	O24	**Serial Port Interrupt Request.** Alternate IRQ output from UART1, refer to CR0 bit 6.
NCSJ DRATE0	19	I O24	**NCSJ.** This pin is used as an input for an external decoder circuit which is used to qualify address lines above all. If this pin is logically ORed with A11-A15, then it can qualify as 16-bit full decoder. If this function is not used, this pin must be connected to ground. As an output function, this pin reflects the bit 0 of the data rate register.
Serial Port Interface			
RXD1, RXD2	78, 88	I	**Receive Data.** Receiver serial data input.
TXD1, PCF0	79	O4 I	**Transmit Data.** Transmitter serial data output from Primary Serial Port. **Parallel Port configuration control 0.** During reset active, this input signal is read and latched to define the address of the Parallel port.
RTS1J RCF1	81	O4 I	**Request to send.** Active low Request to send output for Primary Serial port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTSJ signal to inactive mode (high). Forced inactive during loop mode operation. **Parallel port configuration control 1.** During reset active, this input is read and latched to define the address of the Parallel port.
RTS2J S2CF0	91	O4 I	**Request to send.** This active low output for Secondary Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTSJ signal to inactive mode (high). Forced inactive during loop mode operation. **Secondary serial port configuration control 0.** During reset active, this input is read and latched to define the address of the Secondary serial port.
DTR1J ECPEN0	83	O4 I	**Data Terminal Ready.** This is an active low output for primary serial port. Handshake output signal signifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTRJ signal to inactive during loop mode operation. **Enhanced parallel port mode seject.** Read and latched during reset active.
DTR2J S2CF1	93	O4 I	**Data Terminal Ready.** This active low output is for secondary serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTRJ signal to inactive mode (high). Forced inactive during loop mode operation. **Secondary serial port configuration control 1.** When active, this input is read and latched to define the address of the Secondary Serial port.
FXD2 FDCCF	89	O4 I	**Transmitter Serial Data output from Secondary Serial Port.** **Floppy Disk Configuration.** This input is read and latched during Reset to enable/disable the Floppy Disk Controller.
CTS1J CTS2J	82, 92	I	**Clear to Send.** This active low input for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of CTSJ signal by reading bit 4 Modem status Register (MSR). A CTSJ signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when CTSJ changes state. The CTSJ signal has no effect on the transmitter. Note: Bit 4 of MSR is the complement of CTSJ.
DSR1J DSR2J	80, 90	I	**Data Set Ready.** This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of DSRJ signal by reading bit 5 of Modem Status Register (MSR). A DSRJ signal state changes from low to high after the last MSR read sets MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DSRJ changes state. **Note:** Bit 5 of MSR is the complement of DSRJ.
DCD1J, DCD2J	85, 87	I	**Data Carrier Detect.** This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of DCDJ signal by reading bit 7 of Modem Status Register (MSR). A DCDJ signal state changes from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the Interrupt is generated when DCDJ changes state. Note: bit 7 of MSR is the complement of DCDJ.
RI1J, RI2J	84, 86	I	**Ring Indicator.** This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of RIJ signal by reading bit 6 of Modem Status Register (MSR). An RIJ signal state change from, low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when RIJ changes state. Note, bit 6 of MSR is the complement of RIJ.

Name	Number	Type	Description
DRV2	94	I	**Drive 2.** In PS/2 mode, this input indicates whether a second drive is connected: this signal should be low if a second drive is connected. This status is reflected in a read of Status Register A.
ADRxJ		O24	**Optional I/O port address decode output.** Defaults to tri-state after power-up. This pin has 30 µA internal pull-up. This interrupt from the parallel port enabled/disabled via bit 4 of the
TR2		O24	**Parallel Port Control Register.** Refer to Configuration Registers CRC for more information.
ECPEN1		I	**Enhanced parallel port mode select.** Read and latched during reset active.
SLCTINJ	73	O20	**Printer select input.** This active low signal selects the printer. This is the complement of bit 3 of the Printer Control Register.
INITJ	74	O20	**Initiate Output.** This active low signal is bit 2 of the printer control register. This is used to initiate the printer when low.
AUTOFDJ	76	O20	**Autofeed Output.** This active low output causes the printer to automatically feed one line after each line is printed. This signal is the complement of bit 1 of the Printer Control Register.
STROBEJ	77	O20	**Strobe Output.** This active low pulse is used to strobe the printer data into the printer. This output signal is the complement of bit 0 of the Printer Control Register.
BUSY	61	I	**Busy.** This signal indicates the status of the printer. A high indicates the printer is busy and not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input.
ACKJ	62	I	**Acknowledge.** This active low output from the printer indicates it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the ACKJ input.
PE	60	I	**Paper End.** This signal indicates that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input.
LCT	59	I	**Printer Selected Status.** This active high output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input.
ERRORJ	75	I	**Error.** This active low signal indicates an error condition at the printer.
PD0-PD7	71-68, 66-63	I/O20	**Port Data.** This bi-directional parallel data bus is used to transfer information between CPU and peripherals.
IOCHRDY	100	OD24	**IOCHRDY.** In EPP mode, this pin is pulled low to extend the read/write command.
DRQA/	23	O24	**DMA Request.** Alternate DMA request output for parallel port. Refer to CR5 bit 3.
SICF1		I	**Primary Serial Configuration 1.** Read and latched during reset active to select the address of the Primary Serial Port.
PINTR3/	24	O24	**Parallel Port Interrupt Request.** Alternate IRQ output from Parallel Port. Refer to CR0 bit 4 for more information.
SICF0		I	**Primary Serial Configuration 0.** Read and latched during reset active to define the address of the Primary Serial Port.
IRTX2	25	O4	**Alternate IR Transmit output.**
CFG2		I	This pin is read and latched during reset active to select the hardware configuration port. This pin is internal pull high. If it is low during reset, the hardware configuration port defaults to 3F1h. If it is high during reset, the hardware configuration port defaults to 398h.
IRRX2	26	I	**Alternate IR Receive input.**
FACF			Floppy Disk Address Control. This signal is read and latched during reset active.
UR2IRQB	22	O24	**Serial Port Interrupt Request.** Alternate IRQ output from UART2, refer to CR0 bit 5.
Miscellaneous			
PWRGD	58	I	**Power Good.** This input signal indicates that the power is valid. For device operation, PWRGD must be active.
X1/CLK1	20	ICLK	**Clock 1.** This external connection for a parallel resonant 24 MHz crystal. ACMOS compatible oscillator is required if crystal is not used.
X2/CLK2	21	OCLK	**Clock 2.** This is a 24 MHz crystal. If an external clock is used, this pin should not be connected. This pin should not be used to drive any other drivers.
Vcc	15, 72	P	**Power.** +5 Volt supply pin.
Vss	6, 47, 67, 95	P	**Ground pins.**

Type Descriptions:

I	Input TTL compatible
IS	Input with Schmitt Trigger
I/O20	Input/Output with 16 mA sink @ 0.4 V, source 16 mA @ 2.4 V
I/O24	Input/Output with 24 mA sink @ 0.4 V, source 12mA @ 2.4 V
I/O36	Input/Output with 36 mA sink @ 0.4 V, source 8 mA @ 2.4 V
ICLK	CLK input at 24 MHz
OCLK	CLK output at 24 MHz
O4	Output with 4 mA @ 0.4 V, source 4 mA @ 2.4 V
O16	Output with 16 mA sink @ 0.4 V, source 8 mA @ 2.4 V
O20	Output with 16 mA sink @ 0.4 V, source 16 mA @ 2.4 V
O24	Output with 24 mA sink @ 0.4 V, source 12 mA @ 2.4 V
O36	Output with 36 mA sink @ 0.4 V, source 8 mA @ 2.4 V
OD24	Open drain outputs, sinks 24 mA @ 0.4 V
OD36	Open drain outputs, sinks 36 mA @ 0.4 V

11-4. Functional block diagram



12. System Controller 2

12-1. PSC2 Feature Outline

Sharp's LZ9A10000 is used as the PSC2, controlling the devices connected to the ISA bus.

BIOS ROM control

MASK ROM control

ROM and RAM disk control

The PSC2 internally expands dedicated interrupts to allow ISA interrupts to be assigned.

Incorporated DOS convertible UART2 channel

Incorporated UART2 channel for VFD I/F

Incorporated UART1 channel for touch panel

Incorporated 2 channels of MCR I/F

Incorporated 4 channels of drawer I/F

Incorporated 2 channels of CKDC I/F

Incorporated mode key I/F and clerk key I/F

Supported input ports of system SW

Incorporated 2 channels of 8-bit timer counter

Decoded output of super I/O upper address

Reset control

12-2. Memory Control

12-2-1. BIOS ROM Control

Up to 512K bytes of flash ROM memory with 16-bit configuration can be used as BIOS ROM. The interface is designed to be connected to the ISA bus.

The PSC2 outputs address A18 signal to the BIOS ROM. So when setting the BIOS ROM area to C0000H to FFFFFH using a chip set, this area can be accessed in 256K bytes.

12-2-2. MASK ROM Control

Up to 4M bytes of mask ROM memory with 16-bit configuration can be used as mask ROM. The interface is designed to be connected to the ISA bus. The specifications of decoding is as the following table, so MROMCS# signal is generated.

12-2-3. FLASH ROM Control

Up to 8M bytes of flash ROM memory with 16-bit configuration can be used as flash ROM. The interface is designed to be connected to the ISA bus.

FROS0# area:

Bank base address + 000000H to 003FFFH Bank 200H to 27FH

FROS1# area:

Bank base address + 000000H to 003FFFH Bank 280H to 2FFH

FROS2# area:

Bank base address + 000000H to 003FFFH Bank 300H to 37FH

FROS3# area:

Bank base address + 000000H to 003FFFH Bank 380H to 3FFH

12-2-4. RAM Disk Control

Up to 8M bytes of PS RAM with 16-bit configuration can be controlled as a RAM disk. The interface is designed to be connected to the ISA bus.

PRAS0 area:

Bank base address + 004000H to 007FFFH Bank 000H to 03FH

PRAS1 area:

Bank base address + 004000H to 007FFFH Bank 040H to 07FH

PRAS2 area:

Bank base address + 004000H to 007FFFH Bank 080H to 0BFH

PRAS3 area:

Bank base address + 004000H to 007FFFH Bank 000H to 1FFH

The refresh control of pseudo SRAM is performed as follows:

Use a refresh cycle to disable the decode output to the pseudo SRAM during the refresh cycle, and output a refresh signal with the speed of about 135ns from the PSC2 to OE#/RFSH# of the pseudo SRAM. So the pseudo SRAM can be refreshed automatically without taking the arbitration with other bus masters into consideration.

After power off (POFF#="0") is detected, if the power down of DC 5V (PWRGOOD="0") is detected or 200ms elapsed, PWRGD signal is automatically set to "0" by hardware. Applications must be completely shunted before the PSC2 automatically shutdowns. When resetting using the software, enabling the shutdown enable bit (bit 0 of special system register 1) allows hardware reset. After enabling this bit, the pseudo SRAM goes in self refresh cycle with synchronized with the refresh cycle. After powering up again and REFRESH signal is outputted and stable, disable the shutdown enable bit. Then the pseudo SRAM is refreshed in automatic refresh mode.

12-2-5. BIOS Bank Control

This is a register to set banks in 512K bytes of BIOS ROM. Data set in the BBR0 is outputted from BA18.

12-2-6. Bank Base Address Control

This is a register to set the base address of the ROM and RAM disk bank.

12-2-7. Mask/Flash ROM Bank Control

This is a register to set the bank address of the mask/flash ROM. When bank base address + 0000H to 3FFFH is used as a bank, ROBA8-0 is outputted to BA8-0. ROBA9-7 is used to generate the CS signal of the mask/flash ROM.

12-2-8. PS RAM Bank Control

This is a register to set the bank address of PS RAM. The bank base address + 4000H to 7FFFH is used as a bank. RABA8-0 is outputted to BA8-0. ROBA8-6 is used to generate the CS signal of PS RAM.

12-3. I/O Control

12-3-1. Special System Register

The special system register has a input port reading setup data defining the system configuration of hardware and software, offset register setting a base address to relocatably place each internal register of the PSC2 on the I/O space, COM decode control register, and shutdown register.

This special system register uses fixed I/O address ranging from 07F0H to 07F1H. This address is in the area used by the FDC, however this address is non-selected address of super I/O. So systems using the PSC2 are limited to a system in which address 07F0H to 07F1H is not selected as an address decoded by the FDC, or a system which uses the super I/O chip.

12-3-2. Interrupt Expansion and Assign Control

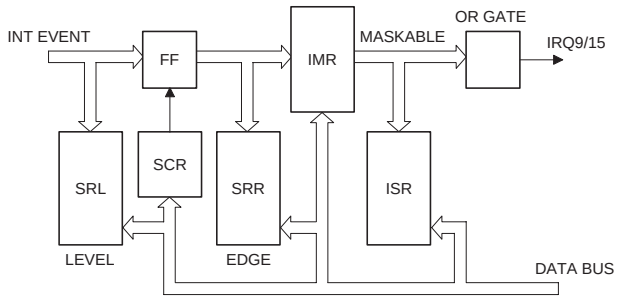
The interrupt control lines on the ISA bus used in the PSC2 are 6 lines: IRQ3, IRQ4, IRQ9, IRQ10, IRQ11, and IRQ15.

Each interrupt control line is outputted by taking OR between signals on the ISA bus and the interrupt signal in the PSC2. UART2 can be assigned to IRQ2, and UART1 can be assigned to IRQ4. PC-X dedicated interrupt (IRQX) can be assigned to IRQ9. UART1, 2, and 5 can be assigned to IRQ10 and 11. UART1/2 and IRQX can be assigned to IRQ15.

IRQX is a signal generated by taking OR among interrupt control from the POS dedicated device.

Assignment to each IRQ is controlled according to the setting of interrupt assign register 0 and 1 (IAR0 and 1).

The PSC2 internal interrupt expansion consists of a maskable interrupt source register (ISR), which is the source of interface OR-composed from each interrupt input, interrupt mask register (IMR) controlling the mask control , status read level register (SRL) reading the status of input which is not masked, status read register (SRR) reading edges, and status clear register (SCR) generating edges for the next interrupt.



IBM-PC's 8259 is programmed based on rising edges and incorporates edge generators on the rear step of each interrupt handling of level input. Edges are generated based on the output of OR-composition when performing dummy writing to the SCR.

The steps generating an edge for general interrupts are as follows:

1) Read the ISR.
2) Check the factor of interrupt.
3) Perform the handling of interrupt for each factor.
4) Write clear the corresponding SCR bit to generate the following edge.

   Read in interrupt disable state and clear the corresponding bit to "1" to write.
5) Return from the interrupt handling.

12-3-3. RS232 Interface

2 UARTs (8250) for RS232 are incorporated in the PSC2 as a Mega Macro Function. UART1 and 2 are decoded as follows by the setting of bit 7 of the SSR0 register.

Bit 7: CMOS (decode control of UART1 and 2)

SW7=1: DOS compatible COM3/COM4 mode (initial value)
COM3: 3E8H to 3EFH (8-byte address)
COM4: 2E8H to 2EFH (8-byte address)

SW7=0: Unique decode mode
Unique: PSC2+410H (16-byte address)
i.e. UART1 unit: PSC2+(410-417H)
UART2 unit: PSC2+(418-41FH)

The assignment of interrupt can be freely defined using system SW6 of special system register 0 and the assign register.

The hardware configuration conforms to the RS232 of AT specifications.

12-3-4. Drawer Interface

The I/O port driving the drawer solenoid is composed of the internal gates of PSC2.

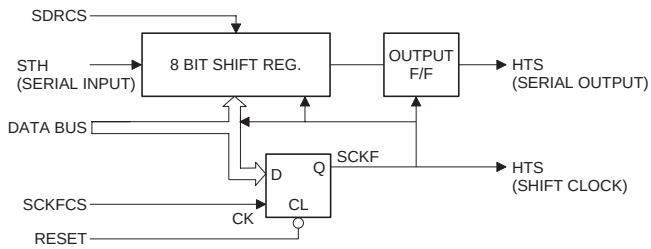
When power off (ACL signal = "0") is detected, each output port is preset and the driving of the drawer solenoid is immediately stopped. The driving time of the drawer solenoid is automatically set to 45ms by the hardware timer control after turning each drive port ON.

12-3-5. CKDC Interface

As previously defined, the CKDC interface, is 2 sets of 8-bit serial interface is incorporated in the PSC2. This interface is composed of an 8-bit parallel-in/parallel-out shift register and a SCKF register for generating shift clock. Also CKDCRES1/2 signals (reset of CKDC) and SHEN1/2# signals (shift enable signal) must be prepared as CKDC interface. However SHEN1/2# are used in the PSC2 as dedicated signal pins inputting interrupt events.

SCKF is outputted to SCK pin without the logic changed and preset to "1" by RESET. The serial data is in the form of LSB first. SCKF operates with synchronized with SCK, and the operation speed depends on the speed of CPU because the shift operation needs to clear and set SCKF by software control for each bit.

STH is shifted in by the rising of SCK, and shifted out by the falling of SCK. The shift-in and shift-out have a margin to the delay of line because of 1/2 bit of phase difference.

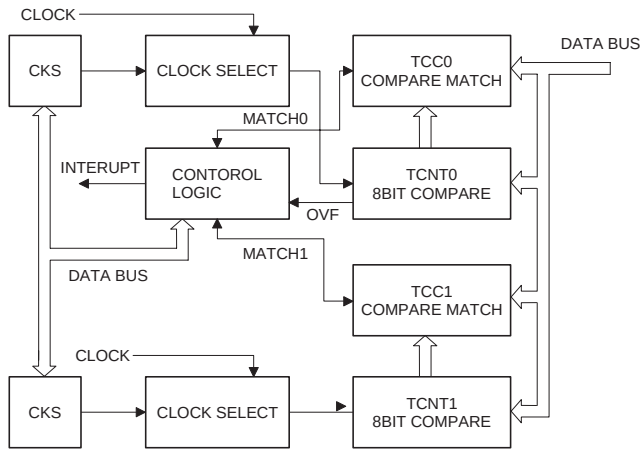


12-3-6. Timer Counter

The PSC2 incorporates 2 8-bit hardware free run counters necessary to control dedicated devices. This 8-bit counter can be read or written as TCNT register 0 and 1, counted up by input clock. This input clock is selected using CLOCK SELECT (2 bits respectively) of the TCR register. When TCNT0 is equal to the value of timer compare constant register (TCC0), compare match signal can be generated and a maskable interrupt can be generated. Also when TCNT1 is equal to TCC1, compare match signal can be generated and a maskable interrupt can be generated. When the TCNT0 overflows, an overflow signal can be generated and a maskable interrupt can be generated.

Types of internal timer interrupt

IS14: TINT0# (timer compare match interrupt 0)
IS13: TINT1# (timer compare match interrupt 1)
IS12: TOINT# (timer overflow interrupt)



12-3-7. MCR Interface

This interface has 2 channels containing 96 bytes of FIFO respectively. Read data are stored in the FIFO. Each channel functions independently, so the 2 channels can be read simultaneously.

Description of Read Operation

1) The MCR interface goes into the status of waiting for reading a card after the following settings are performed by the main CPU.
   - Setting a mode: Sets a mode corresponding to the standard of the handled card (JBA/ABA/IATA).
   - Setting a start mark: Sets a start mark corresponding to the standard of the card.
   - Resetting the interrupt: Resets the interrupt because no card can be read when any interrupt is active.

2) After a card is scanned, the MCR interface changes serial data of the MCR to parallel data. Changed data is written in the FIFO buffer at every character in order from the start mark to the LRC. The FIFO buffer has the capacity of 96 bytes, and the number of characters in a card corresponding to each standard is as follows:

   JBA (JIS II type): 72 characters maximum (8 bits a character)

   ABA (MEGA MACRO FUNCTION II type second track): 40 characters maximum (5 bits a character)

   IATA (JIS I type first track): 79 characters maximum (7 bits a character)

   The 2 FIFOs are prepared independently to 2 channels of interface. These FIFOs can be read simultaneously when connected to a MCR corresponding to JBA/ABA or IATA/ABA.

3) When a card has been scanned, interrupts for the MCR interface are activated.

4) The main CPU reads taken card data from the FIFO buffer in the interrupt handling. The main CPU can read the data using IN command of 0WAIT.

   Even after the LCR which is the last character of a card was read, 10 to 20 characters of "0" remains in the FIFO buffers. So it is necessary to reset the FIFO before read enabling the next card after reading the LCR of the last data.

5) This MCR interface does not read the next card until interrupts are reset by the main CPU.

12-3-8. VFD Interface

The PSC2 has 2 UARTs (8250) as Mega Macro Function. PSC+80XH is used as the I/O address for this interface. Only TXD and DTR are outputted as UART signals from the PSC2.

UART3: PSC2+(800-807H)

UART4: PSC2+(808-80FH)

12-3-9. Analog Touch Panel Interface

The PSC2 has a UART (8250) as Mega Macro Function. PSC+81XH is used as the I/O address for this interface. TXD, RXD, DTR, and CTS are inputted and outputted as UART signals from the PSC2.

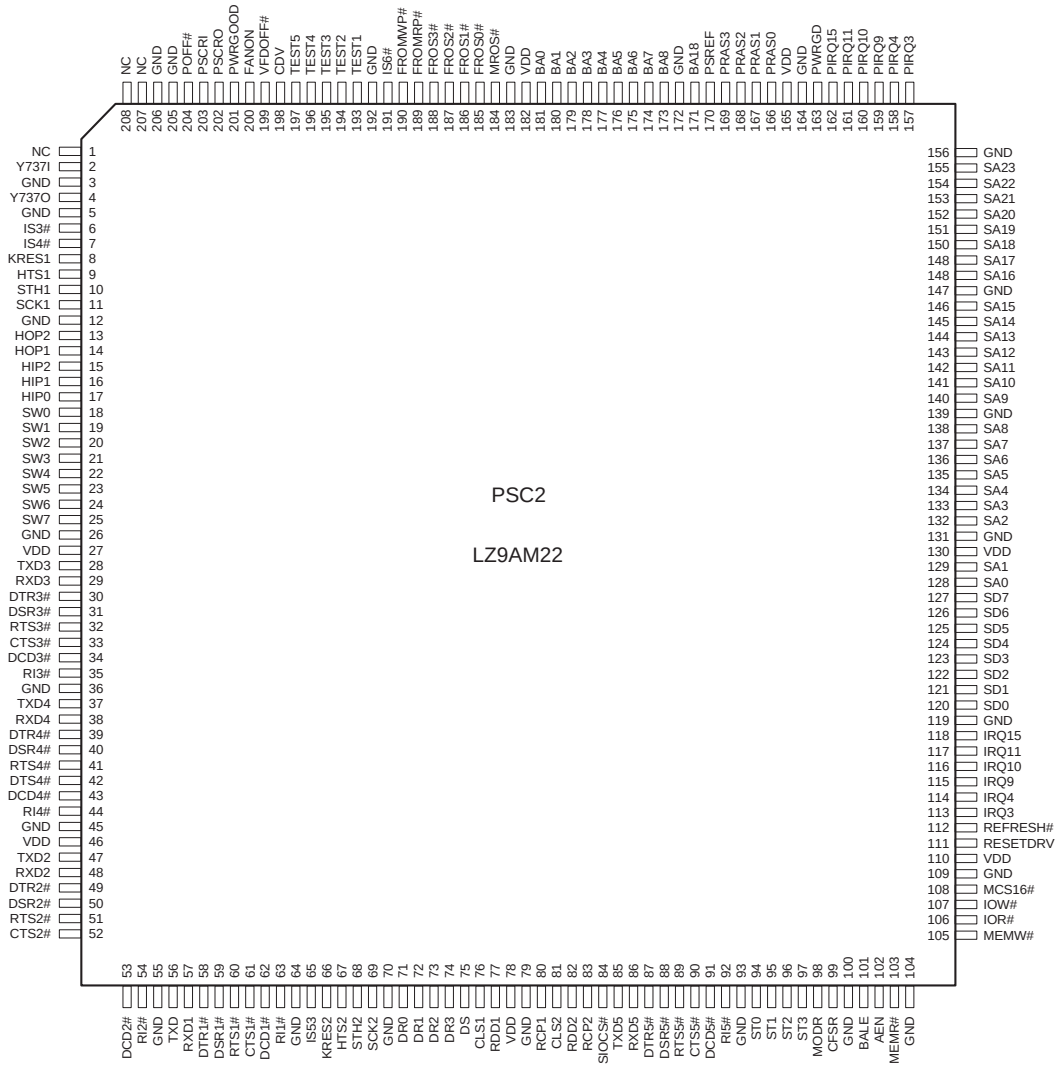
UART5: PSC2+(810-817H)

12-3-10. General Purpose I/O Port

A 6-bit I/O port used for general purposes is configured in the PSC.

12-3-11. Mode Key Control and Clerk Key Control (NotUsed)

12-4. Pin assignment



12-5. Pin description

Pin No.	I/O	Signal name	Function
1		NC	
2	I	Y737I	SERAMIC RESONATOR CLOCK INPUT
3		GND	
4	O	Y737O	SERAMIC RESONATOR CLOCK OUTPUT
5		GND	
6	I	IS3#	STD CKDC INTERRUPT REQUEST (KIRQ1#)
7	I	IS4#	STD CKDC SHIFT ENABLE (SHEN1#)
8	O	KRES1	STD CKDC RESET
9	O	HTS1	STD CKDC HOST TO SUB
10	I	STH1	STD CKDC SUB TO HOST
11	O	SCK1	STD CKDC CLOCK
12		GND	
13	O	HOP2	GENERAL-PURPOSE OUTPUT PORT 2
14	O	HOP1	GENERAL-PURPOSE OUTPUT PORT 1
15	I	HIP2	GENERAL-PURPOSE INPUT PORT 2
16	I	HIP1	GENERAL-PURPOSE INPUT PORT 1
17	I	HIP0	GENERAL-PURPOSE INPUT PORT 0
18	I	SW0	DIP SWITCH 0
19	I	SW1	DIP SWITCH 1
20	I	SW2	DIP SWITCH 2
21	I	SW3	DIP SWITCH 3
22	I	SW4	DIP SWITCH 4
23	I	SW5	DIP SWITCH 5
24	I	SW6	DIP SWITCH 6
25	I	SW7	DIP SWITCH 7
26		GND	
27		VDD	
28	O	TXD3	RS-232 FRONT VFD TXD
29	I	RXD3	RS-232 FRONT VFD RXD
30	O	DTR3#	RS-232 FRONT VFD DTR
31	I	DSR3#	RS-232 FRONT VFD DSR
32	O	RTS3#	RS-232 FRONT VFD RTS
33	I	CTS3#	RS-232 FRONT VFD CTS
34	I	DCD3#	RS-232 FRONT VFD DCD
35	I	RI3#	RS-232 FRONT VFD RI
36		GND	
37	I	TXD4	RS-232 CUSTOMER VFD TXD
38	I	RXD4	RS-232 CUSTOMER VFD RXD
39	O	DTR4#	RS-232 CUSTOMER VFD DTR
40	I	DSR4#	RS-232 CUSTOMER VFD DSR
41	O	RTS4#	RS-232 CUSTOMER VFD RTS
42	I	CTS4#	RS-232 CUSTOMER VFD CTS
43	I	DCD4#	RS-232 CUSTOMER VFD DCD
44	I	RI4#	RS-232 CUSTOMER VFD RI
45		GND	
46		VDD	
47	O	TXD2	RS-232 COM4/6 TXD
48	I	RXD2	RS-232 COM4/6 RXD
49	O	DTR2#	RS-232 COM4/6 DTR
50	I	DSR2#	RS-232 COM4/6 DSR
51	O	RTS2#	RS-232 COM4/6 RTS
52	I	CTS2#	RS-232 COM4/6 CTS
53	I	DCD2#	RS-232 COM4/6 DCD
54	I	RI2#	RS-232 COM4/6 RI
55		GND	
56	O	TXD1	RS-232 COM3/5 TXD
57	I	RXD1	RS-232 COM3/5 RXD
58	O	DTR1#	RS-232 COM3/5 DTR
59	I	DSR1#	RS-232 COM3/5 DSR
60	O	RTS1#	RS-232 COM3/5 RTS
61	I	CTS1#	RS-232 COM3/5 CTS
62	I	DCD1#	RS-232 COM3/5 DCD
63	I	RI1#	RS-232 COM3/5 RI
64		GND	
65	I	IS5#	OPT CKDC SHIFT ENABLE (SHEN2#)
66	O	KRES2	OPT CKDC RESET
67	O	HTS2	OPT CKDC HOST TO SUB
68	I	STH2	OPT CKDC SUB TO HOST
69	O	SCK2	OPT CKDC CLOCK
70		GND	
71	O	DR0	DRAWER DRIVE 0
72	O	DR1	DRAWER DRIVE 1
73	O	DR2	DRAWER DRIVE 2
74	O	DR3	DRAWER DRIVE 3
75	I	DS	DRAWER OPEN SENSOR
76	I	CLS1	MCR CARD LOADING SIGNAL 1
77	I	RDD1	MCR READ DATA 1
78		VDD	
79		GND	
80	I	RCP1	MCR READ CLOCK PULS 1
81	I	CLS2	MCR CARD LOADING SIGNAL 2
82	I	RDD2	MCR READ DATA 2
83	I	RCP2	MCR READ CLOCK PULS 2
84	O	SIOCS#	SUPER I/O A15-A11 DECODE
85	O	TXD5	RS-232 TUCH PANEL TXD
86	I	RXD5	RS-232 TUCH PANEL RXD
87	O	DTR5#	RS-232 TUCH PANEL DTR
88	I	DSR5#	RS-232 TUCH PANEL DSR
89	O	RTS5#	RS-232 TUCH PANEL RTS
90	I	CTS5#	RS-232 TUCH PANEL CTS
91	I	DCD5#	RS-232 TUCH PANEL DCD
92	I	RI5#	RS-232 TUCH PANEL RI
93		GND	
94	O	ST0	MODE KEY/CLERK KEY STROBE 0
95	O	ST1	MODE KEY/CLERK KEY STROBE 1
96	O	ST2	MODE KEY/CLERK KEY STROBE 2
97	O	ST3	MODE KEY/CLERK KEY STROBE 3
98	I	MODR	MODE KEY RETURN
99	I	CFSR	CLERK KEY RETURN
100		GND	
101	I	BALE	ISA BUS ADDRESS LATCH ENABLE from CPU
102	I	AEN	ISA ADDRESS ENABLE from CPU
103	I	MEMR#	ISA MEMORY READ COMMAND from CPU
104		GND	

Pin No.	I/O	Signal name	Function
105	I	MEMW#	ISA MEMORY WRITE COMMAND from CPU
106	I	IOR#	ISA I/O READ COMMAND from CPU
107	I	IOW#	ISA I/O WRITE COMMAND from CPU
108	O	MCS16#	MEMORY CHIP SELECT 16 to CPU
109		GND	
110		VDD	
111	I	RESETDRV	ISA SYSTEM RESET from CPU
112	I	REFRESH#	ISA D-RAM REFRESH from CPU
113	I	IRQ3	ISA INTERRUPT REQUEST 3 from ISA
114	I	IRQ4	ISA INTERRUPT REQUEST 4 from ISA
115	I	IRQ9	ISA INTERRUPT REQUEST 9 from ISA
116	I	IRQ10	ISA INTERRUPT REQUEST 10 from ISA
117	I	IRQ11	ISA INTERRUPT REQUEST 11 from ISA
118	I	IRQ15	ISA INTERRUPT REQUEST 15 from ISA
119		GND	
120	I/O	SD0	ISA BUS D0
121	I/O	SD1	ISA BUS D1
122	I/O	SD2	ISA BUS D2
123	I/O	SD3	ISA BUS D3
124	I/O	SD4	ISA BUS D4
125	I/O	SD5	ISA BUS D5
126	I/O	SD6	ISA BUS D6
127	I/O	SD7	ISA BUS D7
128	I	SA0	ISA BUS SA0
129	I	SA1	ISA BUS SA1
130		VDD	
131		GND	
132	I	SA2	ISA BUS SA2
133	I	SA3	ISA BUS SA3
134	I	SA4	ISA BUS SA4
135	I	SA5	ISA BUS SA5
136	I	SA6	ISA BUS SA6
137	I	SA7	ISA BUS SA7
138	I	SA8	ISA BUS SA8
139		GND	
140	I	SA9	ISA BUS SA9
141	I	SA10	ISA BUS SA10
142	I	SA11	ISA BUS SA11
143	I	SA12	ISA BUS SA12
144	I	SA13	ISA BUS SA13
145	I	SA14	ISA BUS SA14
146	I	SA15	ISA BUS SA15
147		GND	
148	I	SA16	ISA BUS SA16
149	I	SA17	ISA BUS SA17
150	I	SA18	ISA BUS SA18
151	I	SA19	ISA BUS SA19
152	I	SA20	ISA BUS SA20
153	I	SA21	ISA BUS SA21
154	I	SA22	ISA BUS SA22

Pin No.	I/O	Signal name	Function
155	I	SA23	ISA BUS SA23
156		GND	
157	O	PIRQ3	INTERRUPT REQUEST 3 to CPU
158	O	PIRQ4	INTERRUPT REQUEST 4 to CPU
159	O	PIRQ9	INTERRUPT REQUEST 8 to CPU
160	O	PIRQ10	INTERRUPT REQUEST 10 to CPU
161	O	PIRQ11	INTERRUPT REQUEST 11 to CPU
162	O	PIRQ15	INTERRUPT REQUEST 15 to CPU
163	O	PWRGD	POWER GOOD to CPU
164		GND	
165		VDD	
166	O	PRAS0	STD PS RAM WORD CHIP SELECT 0
167	O	PRAS1	OPT PS-RAM WORD CHIP SELECT 1
168	O	PRAS2	OPT PS RAM WORD CHIP SELECT 2
169	O	PRAS3	OPT PS RAM WORD CHIP SELECT 3
170	O	PSREF	PS RAM READ/REFRESH
171	O	BA18	BIOS ROM BASE ADDRESS 18
172		GND	
173	O	BA8	BANK ADDRESS 8
174	O	BA7	BANK ADDRESS 7
175	O	BA6	BANK ADDRESS 6
176	O	BA5	BANK ADDRESS 5
177	O	BA4	BANK ADDRESS 4
178	O	BA3	BANK ADDRESS 3
179	O	BA2	BANK ADDRESS 2
180	O	BA1	BANK ADDRESS 1
181	O	BA0	BANK ADDRESS 0
182		VDD	
183		GND	
184	O	MROS#	MASK ROM CHIP SELECT
185	O	FROS0#	STD FLASH ROM CHIP SELECT
186	O	FROS1#	OPT FLASH ROM 1 CHIP SELECT
187	O	FROS2#	OPT FLASH ROM 2 CHIP SELECT
188	O	FROS3#	OPT FLASH ROM 3 CHIP SELECT
189	O	FROMRP#	FLASH ROM RESET/POWER DOWN
190	O	FROMWP#	FLASH ROM WRITE PROTECT
191	I	IS6#	FLASH ROM READY/BUSY- (FROMBY#)
192		GND	
193	I	TEST1	TEST PIN 1
194	I	TEST2	TEST PIN 2
195	I	TEST3	TEST PIN 3
196	I	TEST4	TEST PIN 4
197	I	TEST5	TEST PIN 5
198	I	CDV	TEST PIN CDV (1:NORMAL 0:TEST)
199	O	VFDOFF#	VFD OFF
200	O	FANON	FAN ON/STANDBY INDICATOR ON-
201	I	PWRGOOD	5V POWER GOOD
202	O	PSCRO	TEST RESET OUT
203	I	PSCRI	TEST RESET IN
204	I	POFF#	ACL INPUT from PS UNIT
205		GND	
206		GND	
207		NC	
208		NC	

13. System switch

13-1. DIP Switch

The PSC2 simply reads switched signals from the DIP switch as hardware. The meaning of DIP switch wholly depends on the software.

: Default setting

DSW-8

Function	OFF (value=1)	ON (value=0)
Serial 3 & 4 decode mode	COM3 & COM4	COM5 & COM6

DSW-7

Function	OFF (value=1)	ON (value=0)
COM3 & COM4 IRQ assign (Serial 3 & 4)	COM3 = IRQ11 COM4 = IRQ10	COM3 = IRQ4 COM4 = IRQ3

DSW-6

Function	OFF (value=1)	ON (value=0)
CMOS Initialize	Not Initialize	Initialize

DSW-5
DSW-4
Drive C:, D: & E: Setting

Drive C:	Drive D:	Drive E:	DSW-4	DSW-5
HDD	—	—	ON (value=0)	ON (value=0)
HDD	PS RAM	Flash ROM	ON (value=0)	OFF (value=1)
PS RAM	Flash ROM	HDD	OFF (value=1)	ON (value=0)
Flash ROM	PS RAM	HDD	OFF (value=1)	OFF (value=1)

DSW-3

Function	OFF (value=1)	ON (value=0)
Boot Drive	Drive A:	Drive C:

DSW-2

Function	OFF (value=1)	ON (value=0)
Drive A: Device	Mask ROM	FDD

DSW-1

Function	OFF (value=1)	ON (value=0)
Floppy Disk Controller	Not Exit	Exit

14. System Memory

14-1. Standard Memory

1,048,576 words × 16 bits DRAM
3.3V single power source (±0.3V)
Access time: 60ns (Maximum)
EDO page mode
Refresh: 4096 cycles/64ms (15.62us)
CBR (CAS before RAS refresh)
Row × Column: 12 × 8 (asymmetric)
Bank 0

14-2. Option Memory

144-pin small outline DIMM
Size: 8/16/32/MB
3.3V single power source (±0.3V)
Access time: 60ns (Maximum)
EDO page mode
Refresh: 15us
CBR (CAS before RAS refresh)
Bank 1

15. BIOS ROM

15-1. Outline

Sharp's LH28F004SUT-NC80
Composed of erase blocks divided into 16KB even blocks
5V single power source (write, erase, and read)
512K words × 8 bits
40-pin TSOP (TYPE1) 4M bits flash ROM
BIOS ROM area: C0000h to FFFFFh
Bank switch between BIOS area and installer area

15-2. Bank Switch

Banks are switched by issuing address signal BA18 from the PSC2.

16. DOS ROM

16-1. Outline

Sharp's LH535VC
2M words × 16 bits
Access time: 120ns (Maximum)
5V single power source
48-pin TSOP 16M bits mask ROM
Relocatable bank base address: C0000h, C8000h, D0000h, D8000h, E0000h, and E8000h
Bank switch of 16KB blocks: Bank 0 to 255

16-2. Bank Base Address

Address signals are inputted from the ISA bus to determine the ROM disk area to be accessed.
This ROM disk area is base address + (0000h-3FFFh) with the size of 16KB.

16-3. Bank Switch

For ROM bank 0 to 255, chip select and bank switch are performed by issuing address signal BA0-7 and chip select signal MR0# from the PSC2.

17. Flash ROM Disk

17-1. Outline

Sharp's LH28F016SUT-10
Composed of erase blocks divided into 64KB even blocks
5V single power source (write, erase, and read)
1M words × 16 bits
56-pin TSOP 16M bits flash ROM
Relocatable bank base address: C0000h, C8000h, D0000h, D8000h, E0000h, and E8000h
Bank switch of 16KB block: Bank 512 to 895

17-2. Bank Base Address

The ROM disk area to be accessed is determined by inputting address signals from the ISA bus.

The ROM disk area is base address + (0000h-3FFFh) with the size of 16KB.

17-3. Bank Switch

For ROM bank 512 to 895, chip select and bank switch are performed by issuing address signal BA0-6 and chip select signal FROS#0-2 from the PSC2.

18. PS RAM Disk

18-1. Outline

Toshiba's TC51V8512AF-12

3V single power source

512K words × 8 bits

32-pin TSOP 4M bits pseudo static RAM

Relocatable bank base address: C0000h, C8000h, D0000h, D8000h, E0000h, and E8000h

Bank switch of 16KB block: Bank 0 to 191

Refresh: 2048 cycles/32ms (15.625us)

18-2. Bank Base Address

The RAM disk area to be accessed is determined by inputting address signals from the ISA bus.

The RAM disk area is base address + (4000h-7FFFh) with the size of 16KB.

18-3. Bank Switch

Chip select and bank switch are performed by issuing address signal BA0-5 and chip select signal PRAS#0-2 from the PSC2.

19. Analog Touch Panel

19-1. Outline

The analog touch panel is controlled by Fujitsu's control IC N010-0559-V021, and the CPU issues commands to this panel through serial interface.

Light load input type

Communication mode: Full duplex communication mode, serial interface

Transmission rate: 9600 bps

Data transmission method: asynchronous start-stop synchronization

Signal level: TTL level

Data format: Binary

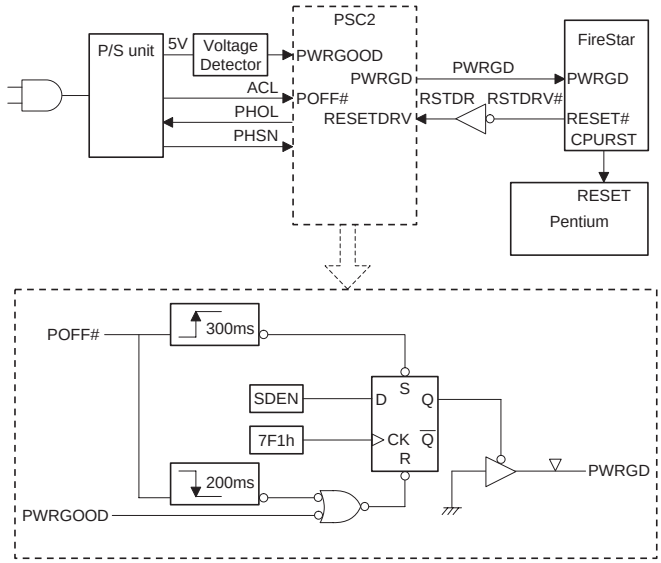
Bit form: Start bit (1) + data bit (8) + stop bit (1), non-parity

Interface signal: RXD/TXD

Sampling speed: 100pps maximum

20. Reset circuit

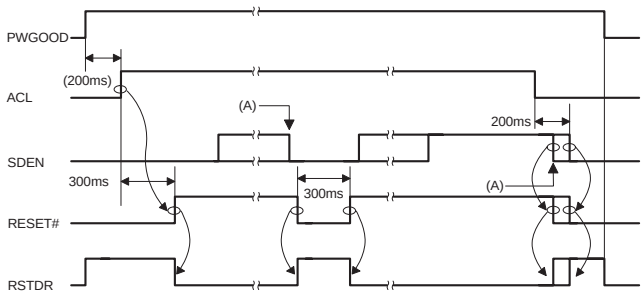
20-1. Block diagram



The RESETDRV in the PSC2 resets the ISA device in the PSC2.

The PHOLD is a control signal turning ON/OFF of AC input by the software. The PHSNS is a sense signal.

20-2. Timing Chart



(A) Power cut: SSR1 07F1h[1]=0 is set.

(B) Power off: SSR1 07F1h[1]=0 is set.

Power supply is assured only for 50ms from the falling of ACL, setting SSR1 07F1h[1]=0 must be performed within 50ms from the falling of ACL. When this operation is not performed and the power supply is active, the PSC2 sets SSR1 07F1h[1]=0 at 200ms after the falling of ACL.

20-3. Control of Power ON/OFF and Register Sensing State of AC SW

General purpose port (PSC+408h)=588h

HIOP	b7	b6	b5	b4	b3	b2	b1	b0
Read	0	0	PHOLD	SLEEP	0	0	PHSNS	MLOCK
Write	0	0	PHOLD	SLEEP	0	0	0	0

Bit 7-6: Not used.

Bit 5: AC power supply hold signal

PHOLD="0": Power is turned off when the AC switch is set OFF.

PHOLD="1": Power continues to be supplied even when the AC switch is set OFF.

The initial value of PHOLD is "0". To prohibit power off by the manual operation of the AC switch, set PHOLD to "1".

When not prohibiting power off by the manual operation of the AC switch, set PHOLD to "0".

PHOLD is designed in order to protect power off by the manual operation of the AC switch, so this signal is not effective for the stop of power supply due to power cut etc.

Bit 4: SLEEP=0 Operation Mode The power fan turns and the power source of LCD back light is connected.

SLEEP=1 Sleep Mode The power fan stops and the power source of LCD back light is disconnected.

Note:
∗ UP-5300 must be always used under SLEEP=0.

Bit 3-2: Not used.

Bit 1: Register sensing the status of AC switch

PHSNS="0": The AC switch is turned OFF.

PHSNS="1": The AC switch is turned ON.

Bit 0: UP-5300 is not used (whether the CPU cooler motor is locked or not is sensed).

(MLOCK=0: The motor is running.)

(MLOCK=1: The motor is not running.)

20-4. Shutdown Control

The power switch of UP-5300 is used to switch the ON state and stand-by state of terminal.

When starting up the terminal, the power switch is necessary to be set ON. When the power switch is set to the position of stand-by mode, the power source unit stops automatically. If HOP1 pin of the PSC2 is held (PHOLD=1) by the software, the power source unit continues to run until the software releases this holding.

If the software can not control shutdown, turning ON the shutdown switch on the side panel can force stand-by mode to be released. However, when the power switch is set ON, turning ON the shutdown switch does not stop the power source unit.

21. Vacuum Fluorescent Display (VFD)

21-1. UP-P20DP/I20DP

21-2. Outline

Content of display: 5 × 7 dots (20 digits × 2 lines) + period + comma + ▽

PSC2 internal UART4 is used as COM8.

(RS-232C level I/F, serial, 8 bits, non-parity, 1 stop-bit, 9600 bps, and RXD/DSR/DTR)

When powering on, the ▽ mark blinks automatically.

21-3. VFD Control

The UART4 incorporated in the PSC2 as Mega Macro Function is used. The I/O address of this interface is PSC2+(808h-80Fh)=988h-98Fh.

21-4. Connector Specifications

RJ45 (for UP-P20DP)

Pin No.	Signal	Function	I/O
1	+5V	+5V	—
2	ER	Data terminal Ready	O
3	SD	Send Data	O
4	SG	Signal Ground	—
5	SG	Signal Ground	—
6	(NC)	(Not Connected)	
7	DR	Data set Ready	I
8	+5V	+5V	O

Connector (for UP-I20DP)

Pin No.	Signal	Function	I/O
1	SG	Signal Ground	—
2	SG	Signal Ground	—
3	SD	Send Data	O
4	ER	Data terminal Ready	O
5	DR	Data set Ready	I
6	+5V	+5V	—
7	+5V	+5V	—

21-5. Cautions

UP-P20DP and UP-I20DP can not be used simultaneously with installed on the same system because of their power capacity.

22. Drawer

22-1. Outline

ER-03DW and ER-04DW, supports 2 channels but only one drive is supported at a time.

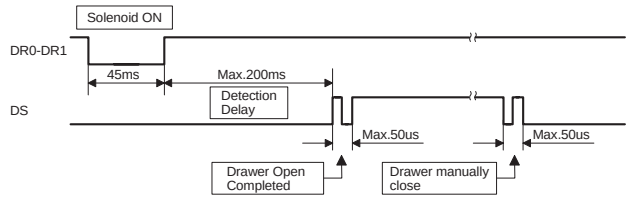
The time in which the drawer is driven by the PSC2 is 45ms.

Time elapsed since the drawer is driven by the PSC2 until DS signal becomes active (sense active time) is 200ms.

Drive shutdown feature depending on detecting power cut in the PSC2.

22-2. Drawer Control

22-3. Timing Chart



23. Magnetic Card Reader (MCR)

23-1. Outline

UP-E12MR2 is the suggested MCR.

UP-E12MR2 supports 2 channels of MCR interface. These 2 channels can be read simultaneously.

96 bytes of FIFO is incorporated in each channel.

23-2. Card Read Operation

1) The MCR interface goes into the status of waiting for reading a card after the following settings are performed by the main CPU.
   (1) Setting a mode:
   Sets a mode corresponding to the standard of the handled card (JBA/ABA/IATA).
   (2) Setting a start mark:
   Sets a start mark corresponding to the standard of the card.
   (3) Resetting the interrupt:
   Resets the interrupt because no card can be read when any interrupt is active.
2) After a card is scanned, the MCR interface changes serial data of the MCR to parallel data. Changed data is written in the FIFO buffer at every character in order from the start mark to the LRC. The FIFO buffer has the capacity of 96 bytes, and the number of characters in a card corresponding to each standard is as follows:
   JBA (JIS 2 type): 72 characters maximum (8 bits a character)
   ABA (JIS 2 type second track): 40 characters maximum (5 bits a character)

IATA (JIS 1 type first track): 79 characters maximum (7 bits a character)

2 FIFOs are prepared independently to 2 channels of interface. These FIFOs can be read simultaneously when connected to a MCR supporting JBA/ABA or IATA/ABA.

3) When a card has been scanned, interrupts for the MCR interface are activated.
4) The main CPU reads card data from the FIFO buffer in the interrupt handling. The main CPU can read the data using IN command of 0WAIT.

   Even after the LCR which is the last character of a card was read, 10 to 20 characters of "0" remains in the FIFO buffers. So it is necessary to reset the FIFO before read enabling the next card after reading the LCR of the last data.
5) This MCR interface does not read the next card until interrupts are reset by the main CPU.

24. Serial Port

24-1. Outline

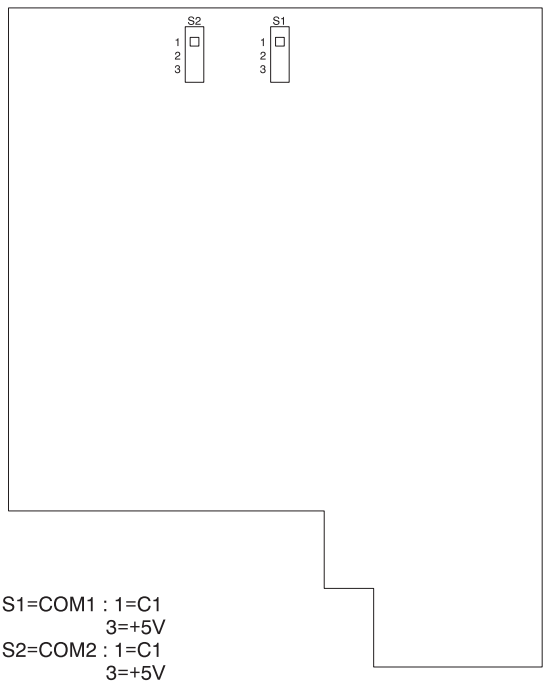
D-SUB 9-pin connector COM1 and COM2 are equipped.

2 channels of RJ45 Connector COM port are equipped.

COM3 and COM4 or original I/O address (COM5 and COM6) can be selected as the 2 channels of RJ45 COM port.

In order to supply +5V power, CI signal and +5V power supply of COM1 and COM2 can be switched.

Main PWB



24-2. Connector Specifications

(1) COM1 & COM2

D-SUB9

Pin No.	Signal	Function	I/O
1	CD	Data Carrier Detect	I
2	RD	Receive Data	I
3	SD	Send Data	O
4	ER	Data Terminal Ready	O
5	SG	Signal Ground	—
6	DR	Data set Ready	I
7	RS	Request to Send	O
8	CS	Clear to Send	I
9	CI/+5V	Ring Indicate/+5V	I/—

(2) COM3/5

RJ45

Pin No.	Signal	Function	I/O
1	RS	Request to Send	O
2	ER	Data terminal Ready	O
3	SD	Send Data	O
4	SG/(+5V)	Signal Ground/(+5V)	—
5	SG	Signal Ground	—
6	RD	Receive Data	I
7	DR	Data set Ready	I
8	CS	Clear to Send	I

Note: +5V can be supplied to pin 4 by switching with a 0Ω resister (By default, pin 4 is used as SG).

(3) COM4/6

RJ45

Pin No.	Signal	Function	I/O
1	RS	Request to Send	O
2	ER	Data terminal Ready	O
3	SD	Send Data	O
4	SG	Signal Ground	—
5	SG	Signal Ground	—
6	RD	Receive Data	I
7	DR	Data set Ready	I
8	CS	Clear to Send	I

CHAPTER 6. BIOS SETUP UTILITY

1. Outline

In the Up-5300, there is an utility that rewrites minimum required setup information at the system bootup which resides in ROM-BIOS.
Setup data is undefined at the first system startup, so setup must be done Basically, system operation can be done just by doing initial setting in setup.
Also, the BIOS in UP-5300 automatically detects memory size / HDD, which makes no need for running setup again after changing hardware (expanding memory, changing HDD, etc).

2. Starting Procedure

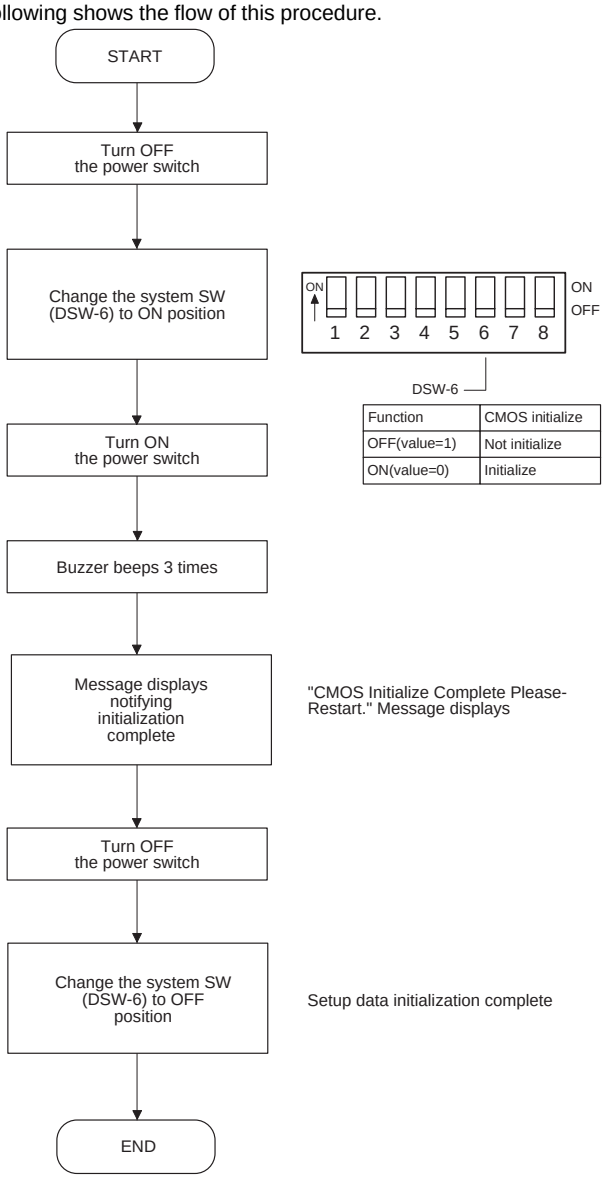
There are 2 ways of starting setup, changing system SW and connecting PS/2 type full keyboard. Setup started by each procedure will be as follows.

Procedure for running setup	Setup contents
Start with system SW	• Setup data initialization
Start with full keyboard	• Setup data initialization • Running setup in menu format

1) Starting setup by changing system SW

Setup data initialization will be processed when system is started with system SW (DSW-6) turned on.

Following shows the flow of this procedure.


START
Turn OFF the power switch
Change the system SW (DSW-6) to ON position
Turn ON the power switch
Buzzer beeps 3 times
Message displays notifying initialization complete
Turn OFF the power switch
Change the system SW (DSW-6) to OFF position
END
ON
OFF
1 2 3 4 5 6 7 8
DSW-6
Function | CMOS initialize
OFF(value=1) | Not initialize
ON(value=0) | Initialize
"CMOS Initialize Complete Please-Restart." Message displays
Setup data initialization complete

2) Starting setup with full keyboard

Starting and operating setup with full keyboard will require PS/2 type full keyboard. Only the num-pad is used to enter setup.

Procedure for starting setup is as follows.

① Start the system.

② Press the following keys according to the type setup desired while SETUP Available message appears on screen.

- Do setup initialization

  On num-pad, press 9 and period at same time.

  Buzzer will beep twice.

- Starting setup in menu format

  On num-pad, press 7 and period at same time.

  After 1 long beep, menu will be displayed.

③ The system will reset automatically after setup is terminated.

3. Setup Outline in Menu Format

The setup in menu format is not required during normal operation. Use only when checking the contents of setup during maintenance, or modifying setup contents required due to system operation.

1) Key assignments

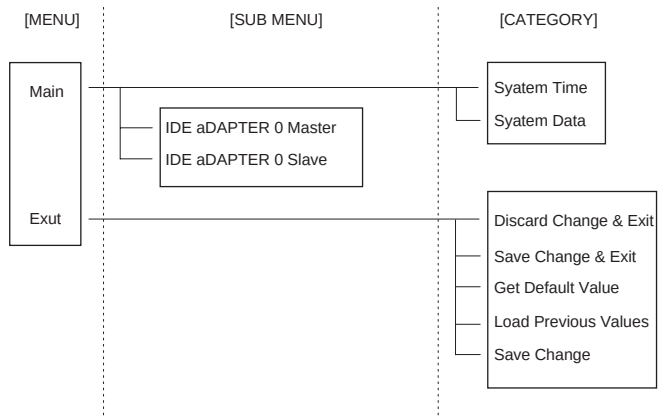
Following num-pad keys are used during operation of setup in menu format.

Key used	Functions
5	Display help
3 (Pg Dn)	Change setting (reverse)
9 (Pg Up)	Change setting (forward)
7 (Home)	Initialize all category displayed
1 (End)	Return to previous value
8 (↑)	Change category (up)
2 (↓)	Change category (down)
4 (←)	Change menu (left)
6 (→)	Change menu (right)
. (Del)	Select submenu, confirm, execute
0 (Ins)	End, return from submenu

Setup in menu format displays key assignment described in lower 2 lines. There is a case that [Continue] and [OK] is displayed while help and in some settings. In this case, press arbitrary key to go to next step. Press period when [Press Enter] is displayed.

4. Menu Tree

Setup menu tree is as follows.



5. Setup Contents in Each Category

[System Time] / [System Date]

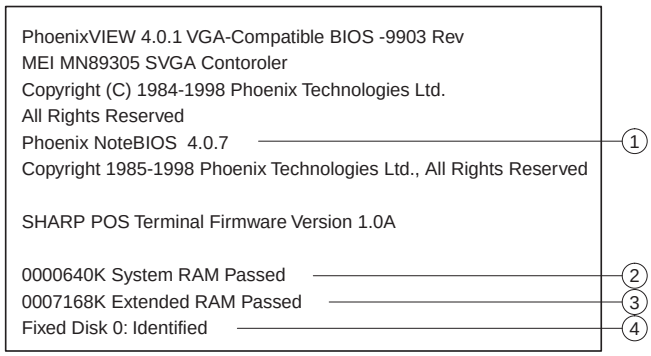
- Configuration for Time / Date in battery backup RTC. Arbitrary Time / Date can be configured.
- If RTC data is undefined, clock is initialized to time 00:00:00 and date 1997-10-01

[IDE Adapter 0 Master] / [IDE Adapter 1 Master]

- Configures HDD type.
- IDE Adapter 0 Master is [Auto], IDE Adapter 1 Master is [None] used for operation.
  For connecting second HDD, set IDE Adapter 1 Master to [Auto]. By setting to Auto, default size of HDD is automatically detected at BIOS bootup.

6. BIOS message on system startup

1) Message on system startup



(1): Sign on message

(2): Message when conventional memory check completes without any errors.

(3): Message when extended memory check completes without any errors.

2) Error message displayed when setup resumes

Following messages are displayed under ④ and below each message, "Setup available" is displayed showing starting setup enabled.

Message	Error meaning
System battery is dead – Replace and run SETUP	Backup cannot be done by lithium battery.
System CMOS checksum bad – run SETUP	Data in CMOS RAM is corrupted
Real time clock error	Configuration in RTC is invalid.

3) Error message displayed when hardware is unusual

Following messages are displayed if hardware is unusual. Following table shows meaning of error messages displayed on different positions.

- Message outputted by system RAM test (position ②)

Message	Error meaning
Nnnn K System RAM Failed at offset:nnnn	W/R error occured in conventional memory at displayed address
nnnn K Shadow RAM Failed at offset:nnnn	W/R error occured in Shadow RAM at displayed address
Failing Bits:nnnn	Bit missing error occured by memory test

- Message displayed by Extended RAM test (position ③)

Message	Error meaning
nnnn K Extended RAM Failed at offset:nnnn	W/R error occured in extended memory at displayed address
Failing Bits:nnnn	Bit missing error occured by memory test

- Message displayed by CPU cache test (position below ③)

Message	Error meaning
System cache error – Cache disabled	Error occured during cash test and disabled cash

- Message displayed by device test (position below ③)

Message	Error meaning
System timer error	Timer chip (8254) error
Keyboard controller error	Error occured during KBC test
Keyboard error	Error occured during full keyboard connection test
Diskette drive A error	FDD error
Incorrect Drive A type – run SETUP	Floppy Disk is not operating normally
Failure Fixed Disk	HDD error
Missing or Invalid NV RAM token	R/W error occured in CMOS RAM

- Message displayed by parity error from bus (position undefined)

Message	Error meaning
Parity Check 1	Parity error (NMI) occured from system bus
Parity Check 2	Parity error (NMI) occured from ISA bus

∗ NOTE

[Message displayed during OS bootup]

Operating system not found

- Boot drive does not exist or OS is not written.
- Make so that OS can be booted and restart the system.

CHAPTER 7. ABOUT UTILITY SOFTWARE AND OTHERS

Two types of UP-5300's utility software are provided by Sharp: one is used on UP-5300, and the other one is used on a PC (personal computer).

1. Utility software used on UP-5300

No.	Software name	File name
1	SYSTEM INSTALLER	Sysins.exe (in Mask ROM disk)

Outline:

The system installer executes automatically on UP-5300 boot up by setting system SW-3 to boot from MROM Disk. It immediately waits for receiving data from host, and processes install by communication command from PC side's installer.
Also, the keyboard operations are not usually required, but by connecting keyboard and operating as needed, communication parameters (COM port / communication baud rate, etc) can be set up. Furthermore, after system installer is terminated, DOS command can be executed by going back to the command prompt. Ex: When HD is connected, execute FDisk / Format and install to HD.

Function:

Following operation can be done.

1. Install POS application and related data files to FROM Disk, PSRAM Disk received from PC connected with RS-232.
2. Connect UP-5300 which is already installed and UP-5300 not installed with RS-232 and copy contents of installed machine to other machine.
3. For optional function, operation such as changing communication configuration, modifying AUTOEXEC.BAT / CONFIG.SYS inside FROM / PSRAM Disk can be done.

No.	Software name	File name
2	Printer LOGO IMAGE LOADING UTILITY	Logo LDUP

Outline:

The printer logo loading utility reads logo image file (Monochrome BMP file) and loads it against ER-01PU or UP-T80BP. To use this utility, the POS device driver must be installed first.
Logo image is written into Flash ROM in the printer.
Loading logo image from application is needed only when changing logo image.

Function:

Loads a logo image to the ER-01PU or UP-T80BP connected to the UP-5300. Also, test printing can be done.
Image file to be loaded is a monochrome bitmap file.

Image data size must be smaller or equal to below list.

	ER-01PU	UP-T80BP
Width (fixed)	360 dot	576 dot
Height(variable, max)	160 dot	240 dot

NOTE: At the ER-01PU, only the receipt side printer can print out the logo data.

No.	Software name	File name
3	TOUCH PANEL CALIBRATION UTILITY PROGRAM	CALDSRP

Outline:

The touch panel calibration utility is used to position the bottom pressing point of touch panel device and to align the LCDs display area.
The adjustment value returned from this utility is saved in EEPROM inside touch panel controller. This will save the data even if the power is shut down.

Function:

At shipment of UP-5300, the touch panel position has already been adjusted.
To adjust it, use the touch pen of K-PDA (Keyboard enhanced Personal Digital Assistant).

PARTS CODE	PARTS NAME	MODEL
CPENP1004PCN5	Touch Pen	K-PDA ZR-xxxx series

2. Utility software used on PC (Personal Computer)

No.	Software name	File name
1	APPLICATION INSTALL PROGRAM (FOR MS-DOS)	APLDDOS

Outline:

POS installer is used to remotely install to the FROM / PSRAM disk on UP-5300 connected by RS-232.

Function:

Following operations can be done.

1. Remote installation of the POS application and related data files into the FROM Disk, PSRAM Disk on the UP-5300 connected via RS-232 cable.

Notice : When installing, contents of the FROM Disk and the PSRAM Disk is erased.

No.	Software name	File name
2	APPLICATION INSTALL PROGRAM (FOR Windows95)	APLDWIN

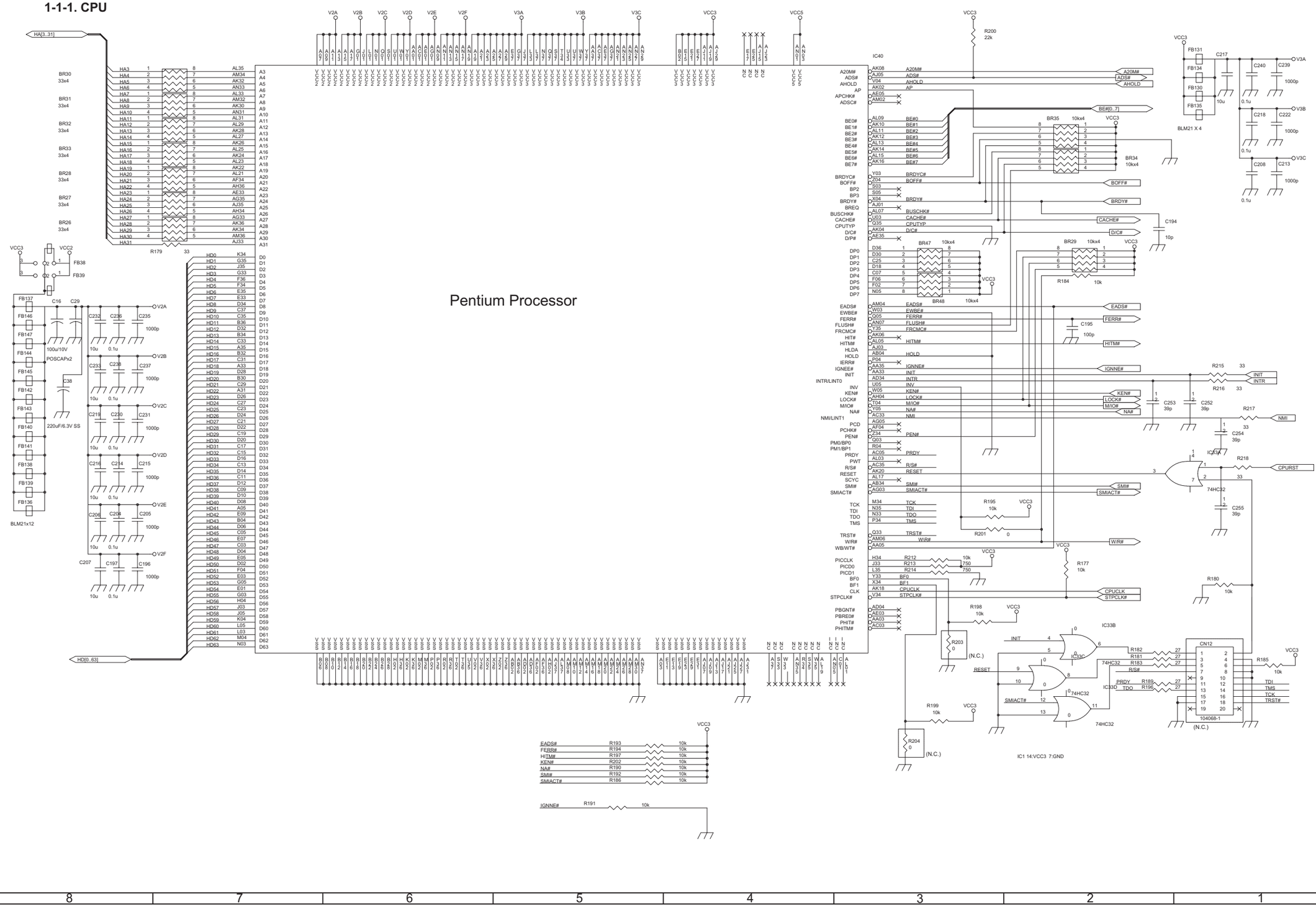
CHAPTER8. CIRCUIT DIAGRAM

(1/6) (1/20)

1. MAIN PWB

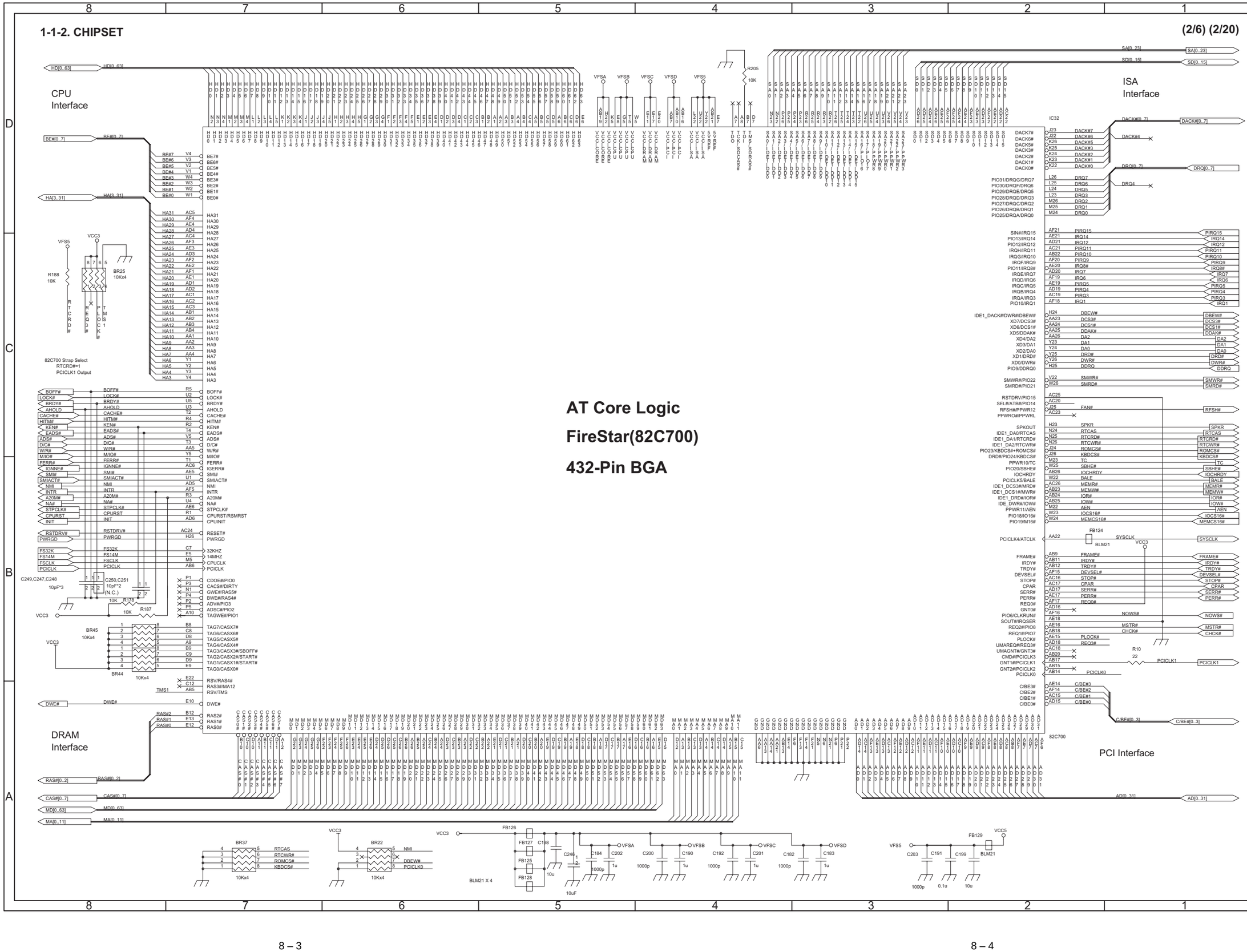
1-1. PC (1/6 -6/6) (1/20 - 6/20)

1-1-1. CPU



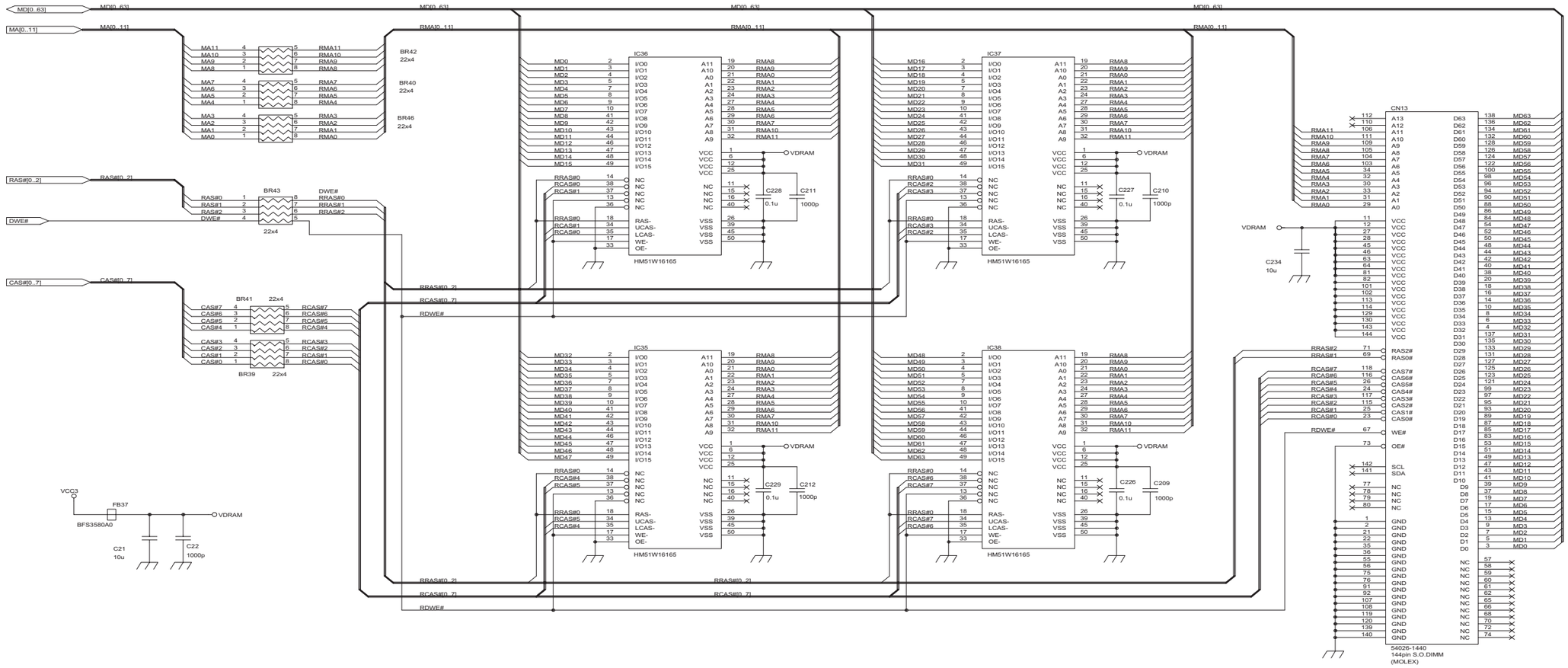
1-1-2. CHIPSET

(2/6) (2/20)



1-1-3. SYSTEM MEMORY

(3/6) (3/20)



1-1-4. KBC & IDE I/F

(4/6) (4/20)

KEY Controller

IC17

M38802M2
64pin TQFP

CN10
52030-1210

CN2
52030-1610
MOLEX

IDE

CN108
A3E-44PA-2DSA

IC29A 74LS125

IC29B 74LS125

IC29C 74LS125

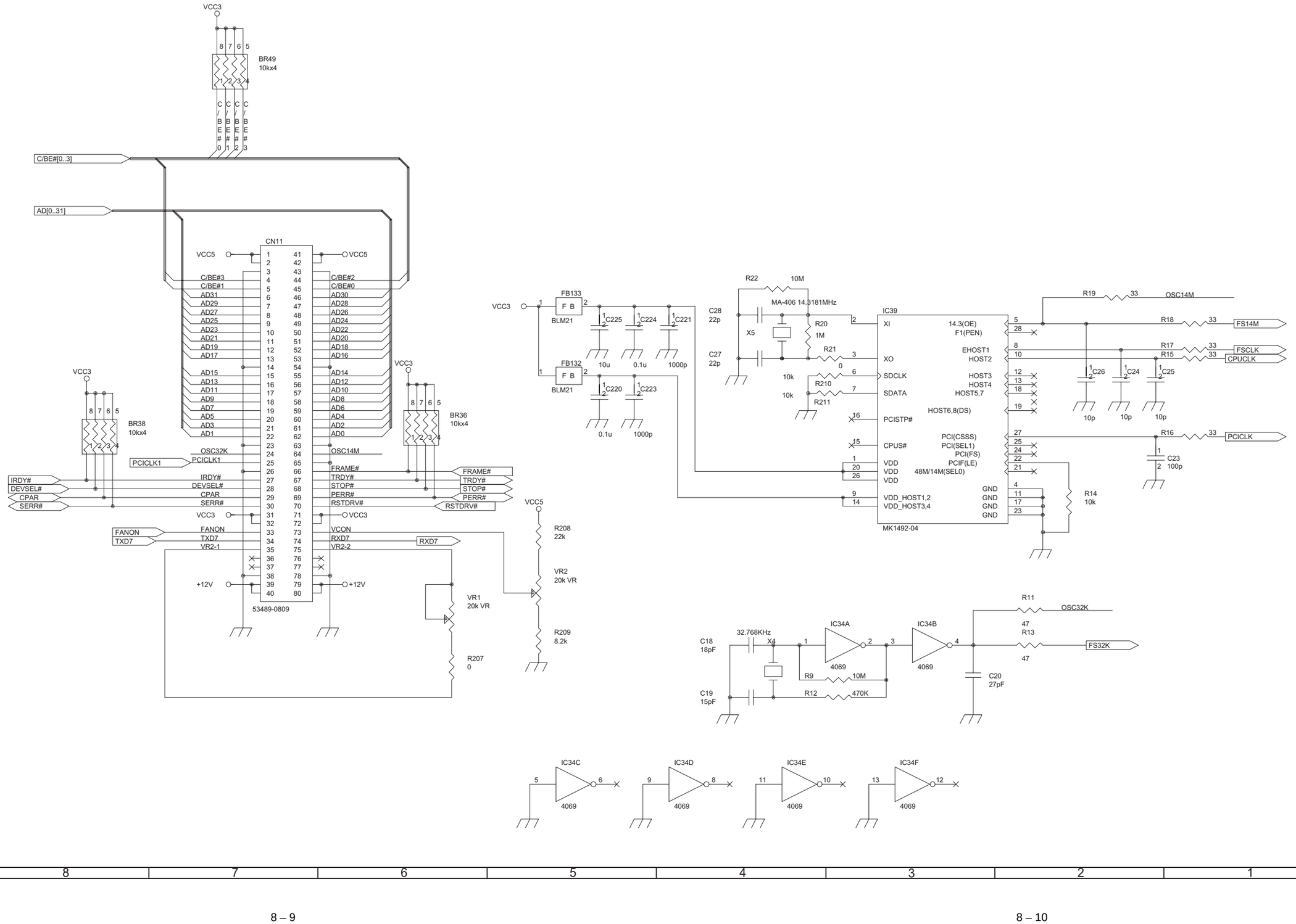
IC29D 74LS125

IC16B 74HC04

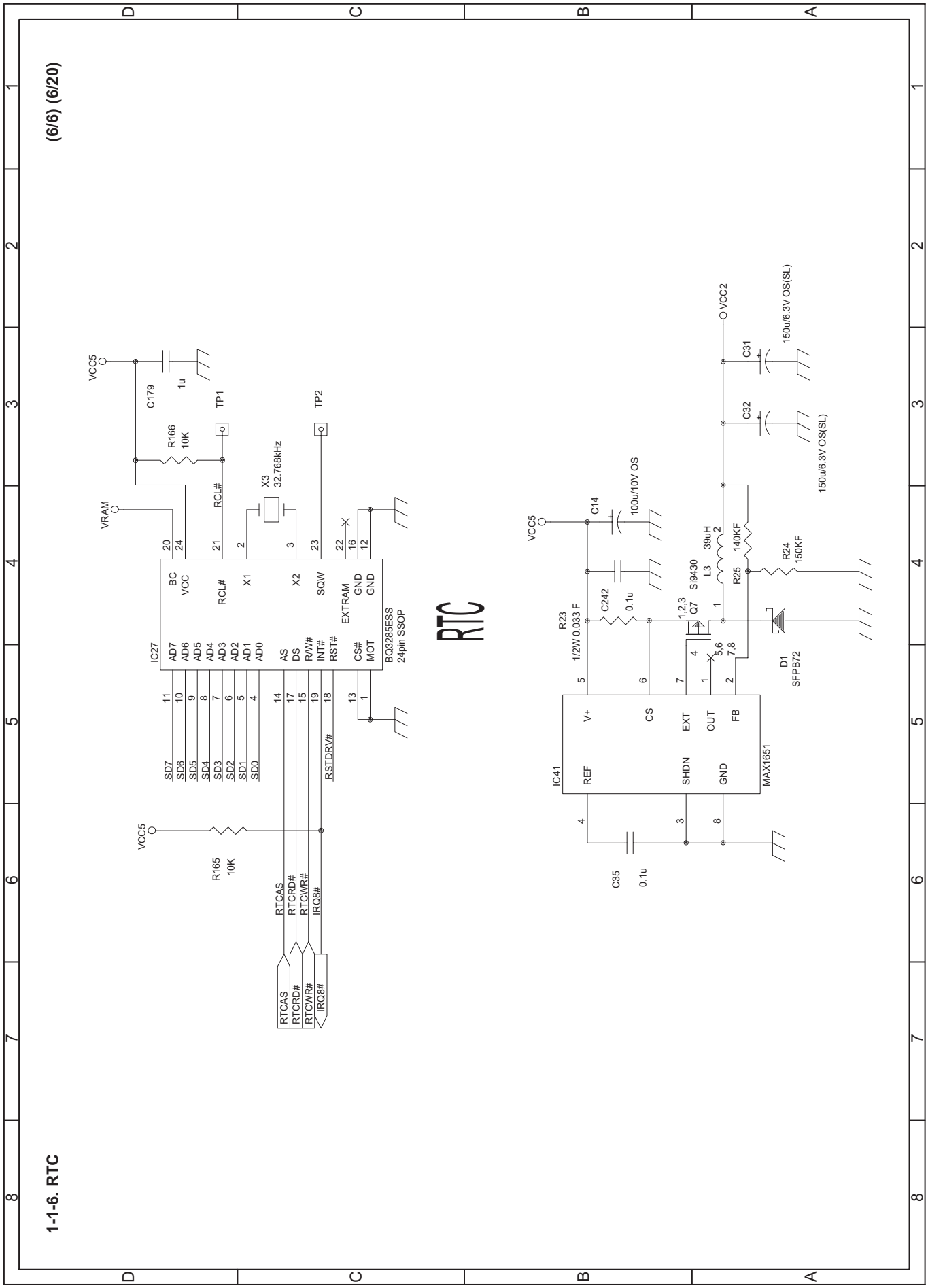
IC16F 74HC04

1-1-5. VGA CONNECTOR

(5/6) (5/20)



(6/6) (6/20)

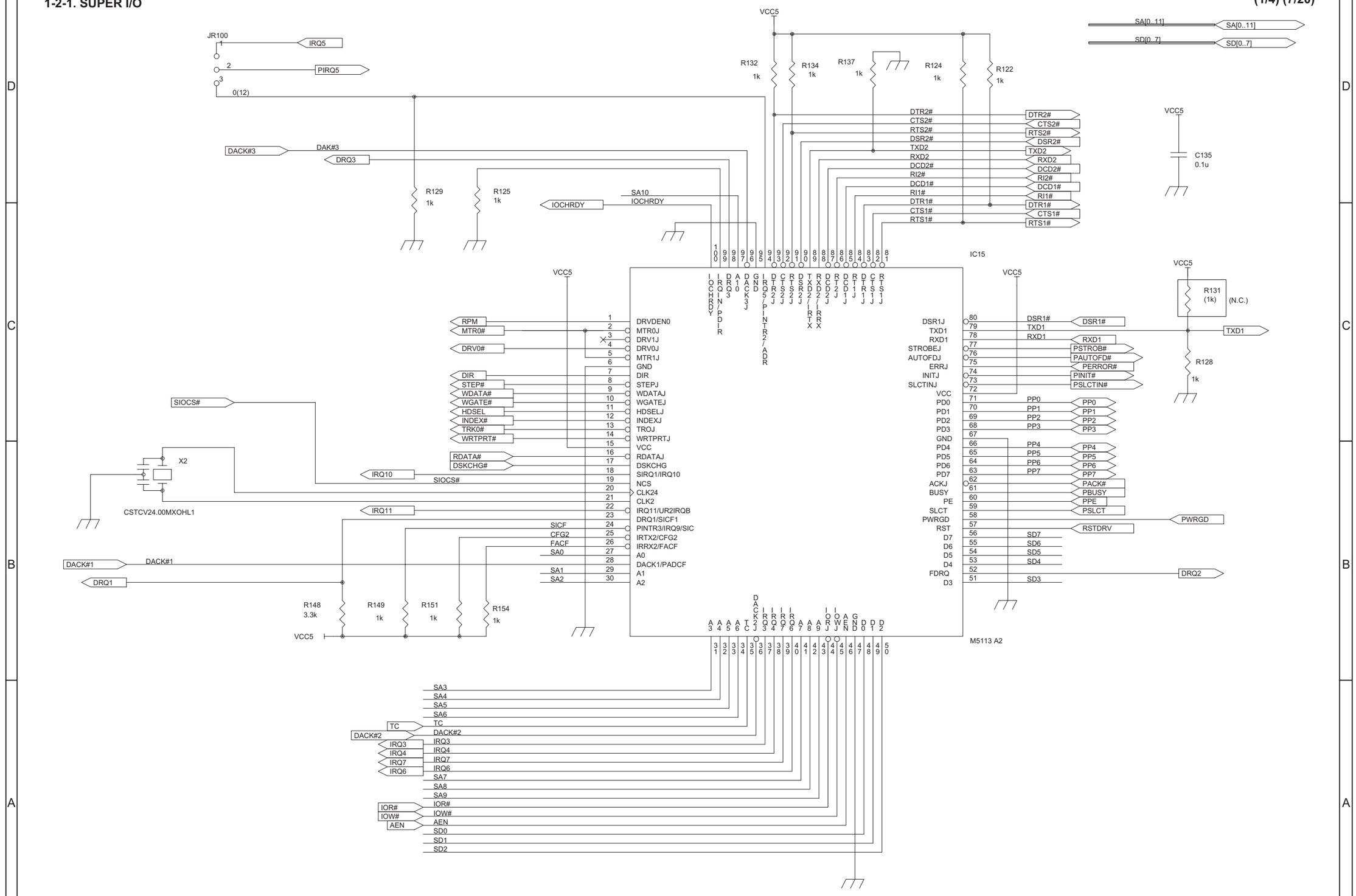


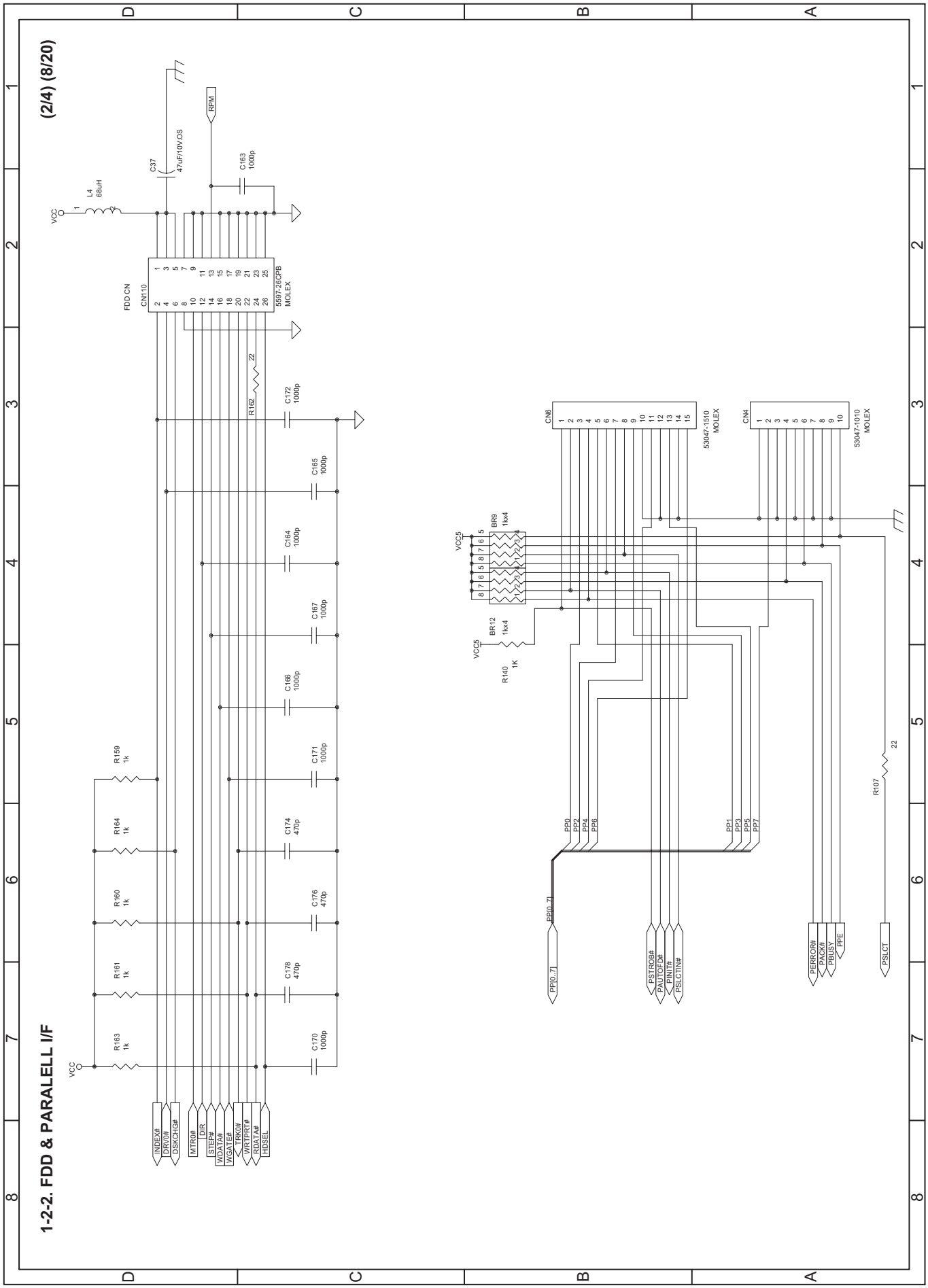
1-1-6. RTC

1-2. ISA STANDARD (1/4 - 4/4) (7/20 - 10/20)

1-2-1. SUPER I/O

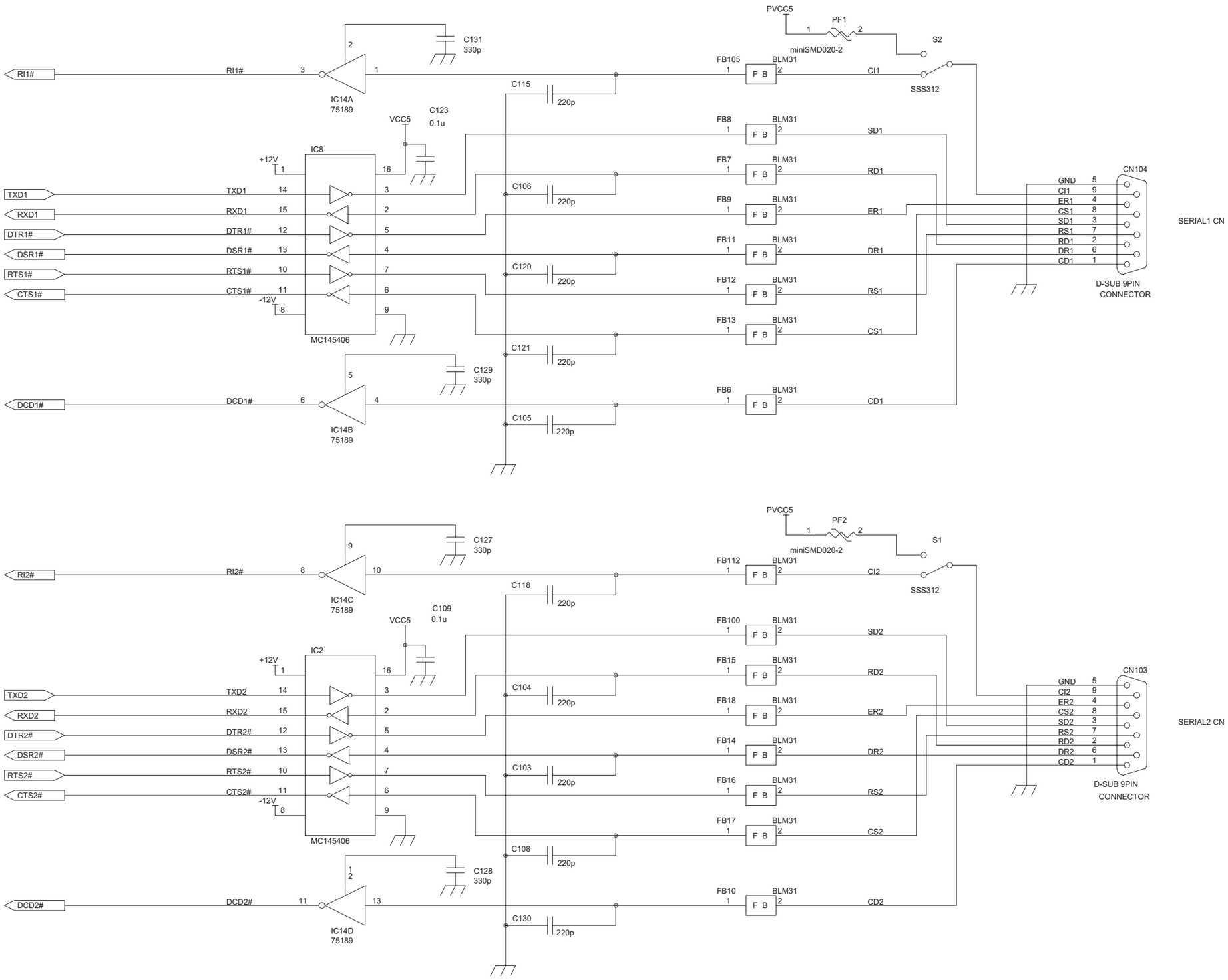
(1/4) (7/20)




(2/4) (8/20)
1-2-2. FDD & PARALELL I/F
FDD CN
CN110
5597-26GPB
MOLEX
L4
68uH
C37
47uF/10V.OS
C163
1000p
RPM
R162
22
C172
1000p
C165
1000p
C164
1000p
C167
1000p
C166
1000p
C171
1000p
C174
470p
C176
470p
C178
470p
C170
1000p
R159
1k
R164
1k
R160
1k
R161
1k
R163
1k
INDEX#
DRVEN#
DSKCHG#
MTR0#
DIR
STEP#
WDATA#
WGATE#
TRK0#
WRTPRT#
RDATA#
HDSEL
CN6
53047-1510
MOLEX
CN4
53047-1010
MOLEX
BR9
1kx4
BR12
1kx4
R140
1K
PP0
PP2
PP4
PP6
PP1
PP3
PP5
PP7
PP[0..7]
PSTROB#
PAUTOFD#
PINIT#
PSLCTIN#
PERROR#
PACK#
PBUSY
PPE
R107
22
PSLCT

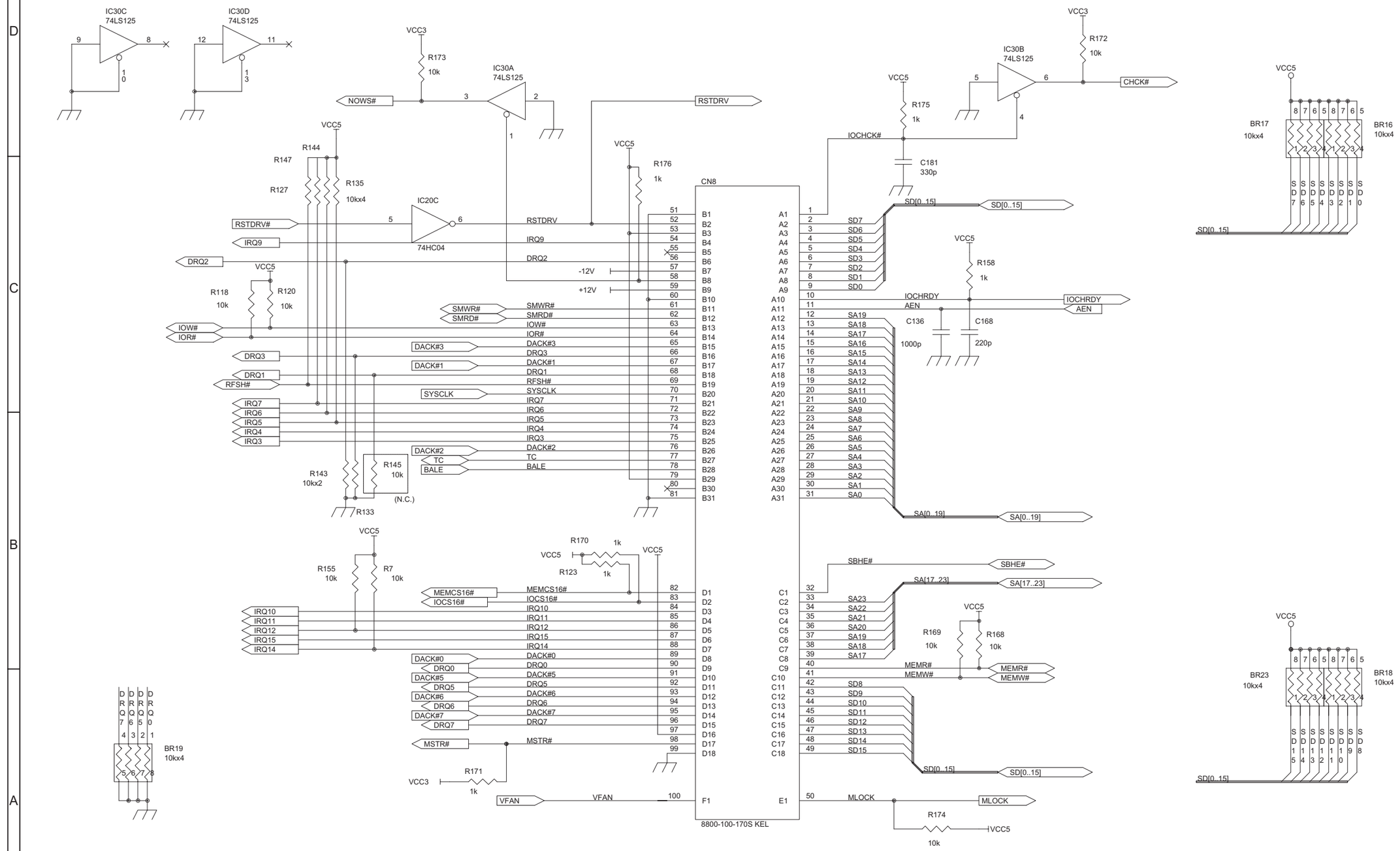
1-2-3. SERIAL 1 & 2

(3/4) (9/20)



1-2-4. SLOT

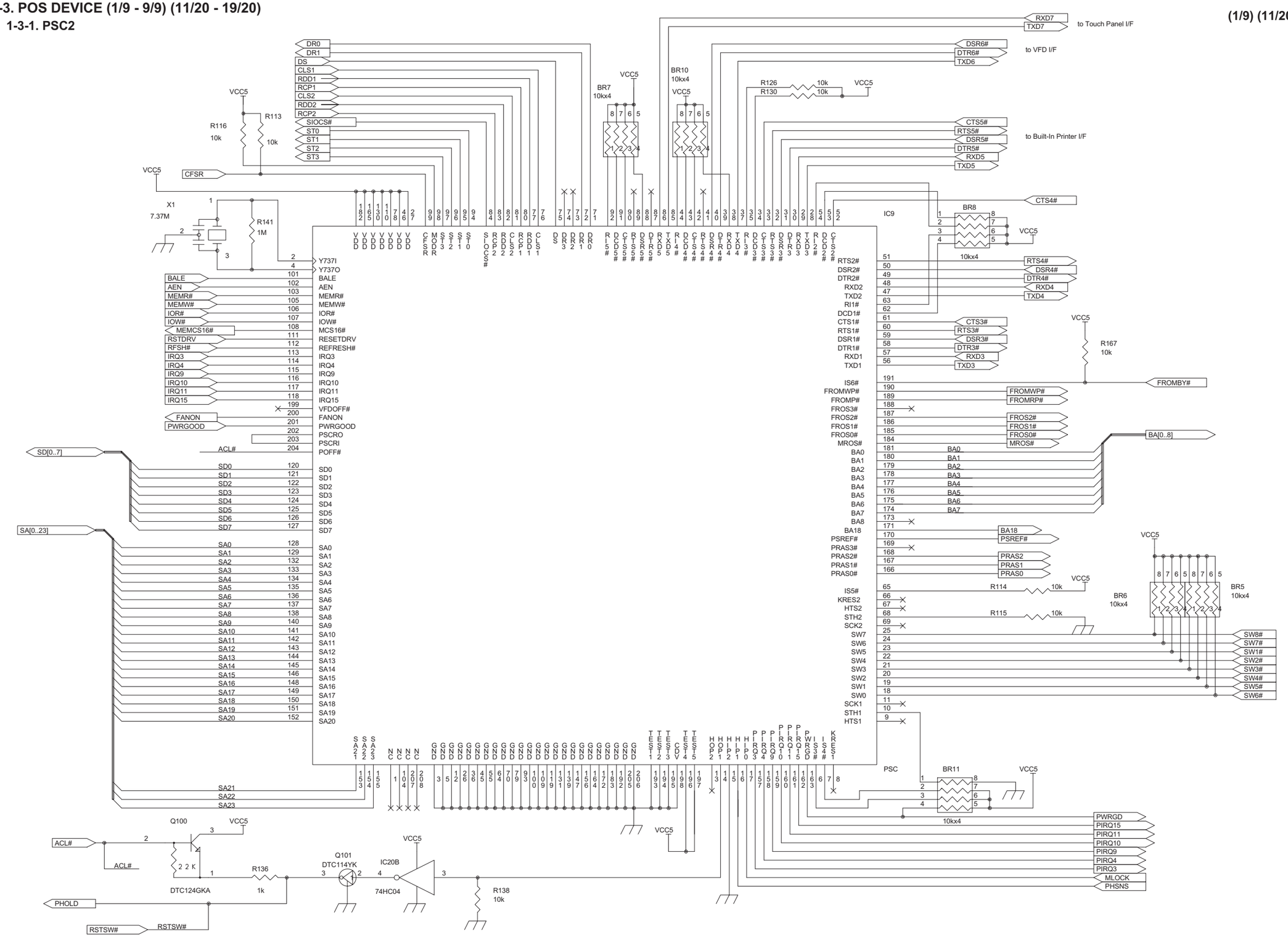
(4/4) (10/20)



1-3. POS DEVICE (1/9 - 9/9) (11/20 - 19/20)

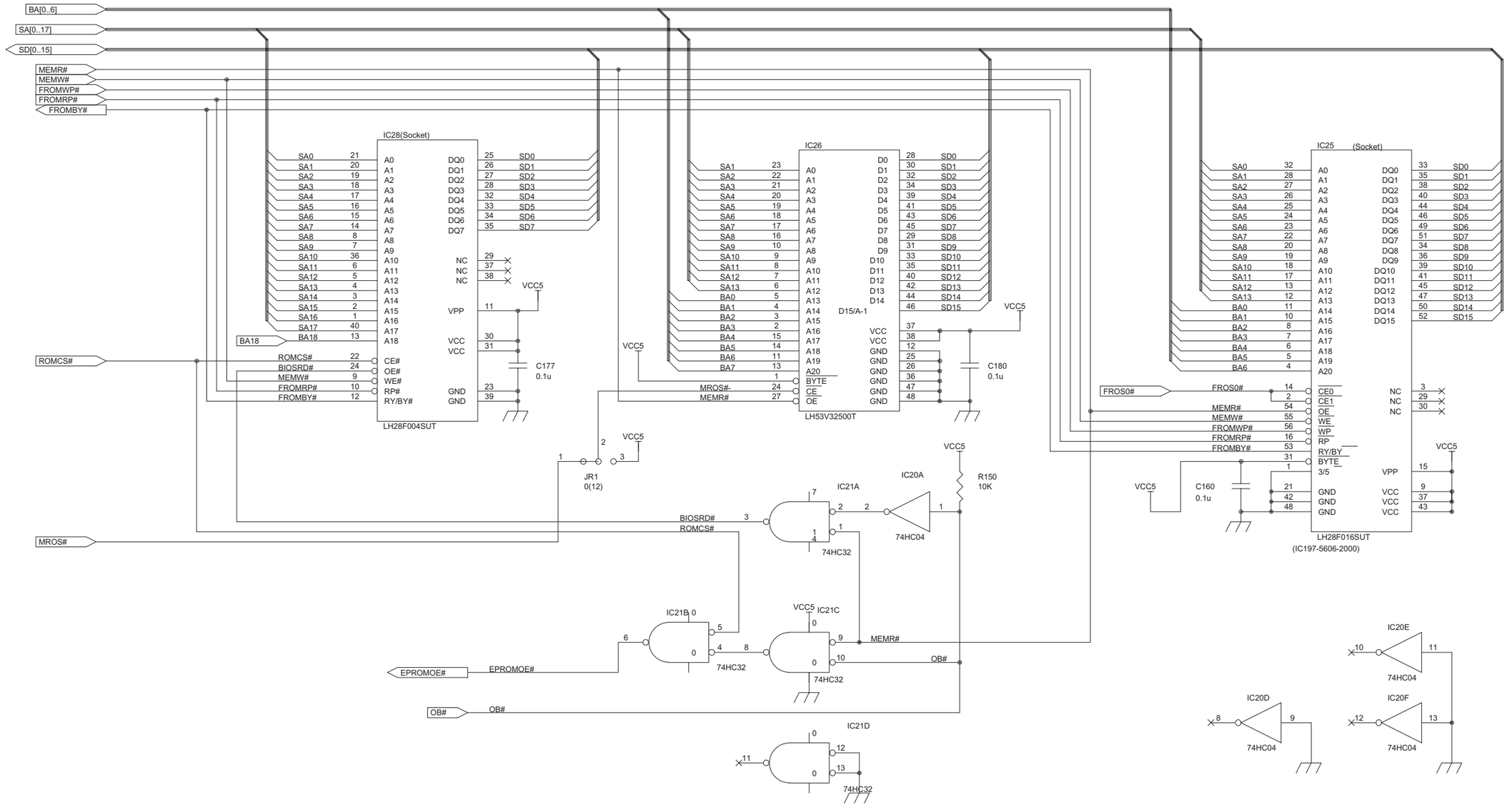
1-3-1. PSC2

(1/9) (11/20)



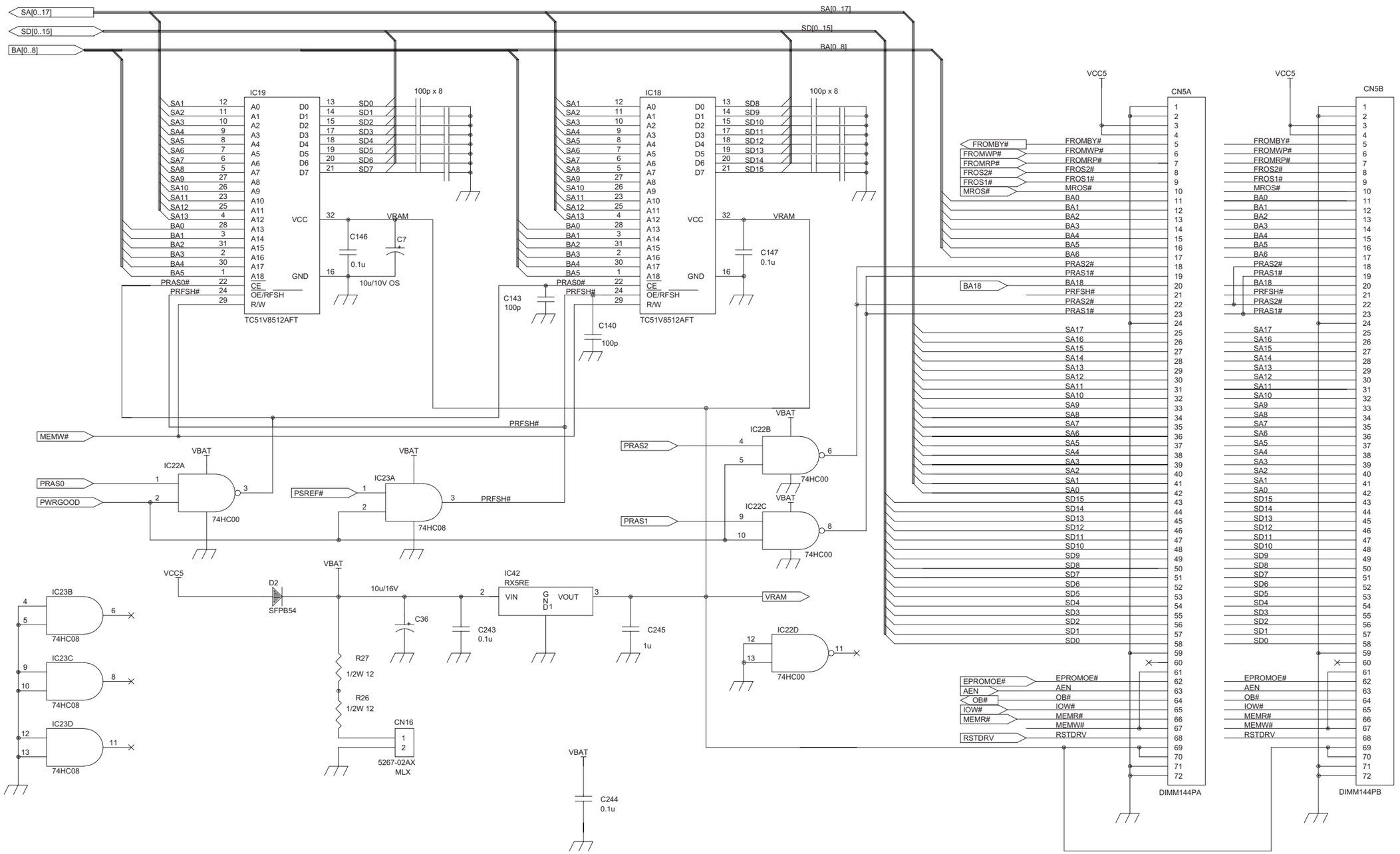
1-3-2. BIOS / DOS / ROM DISK

(2/9) (12/20)

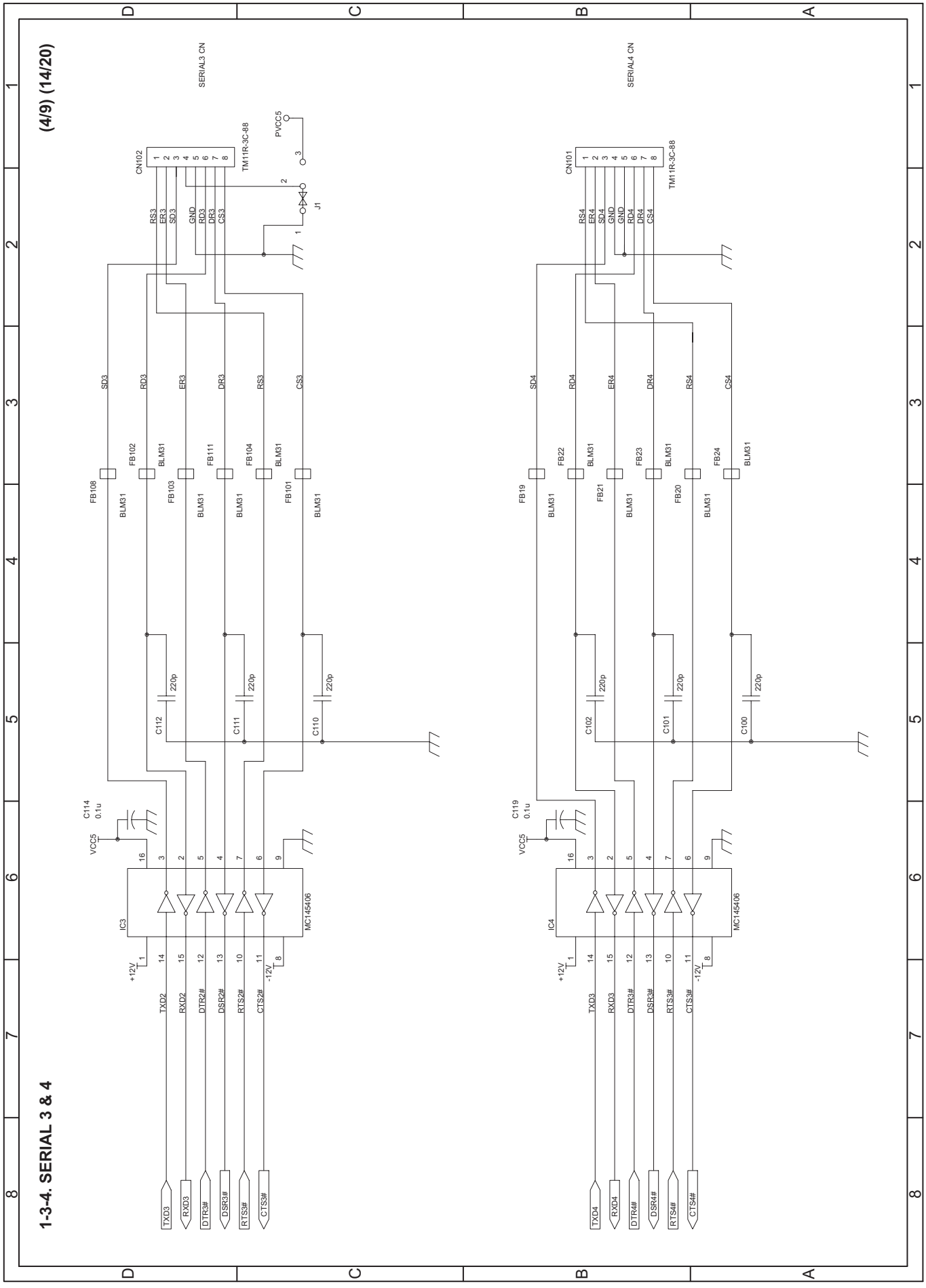


1-3-3. RAM DISK

(3/9) (13/20)

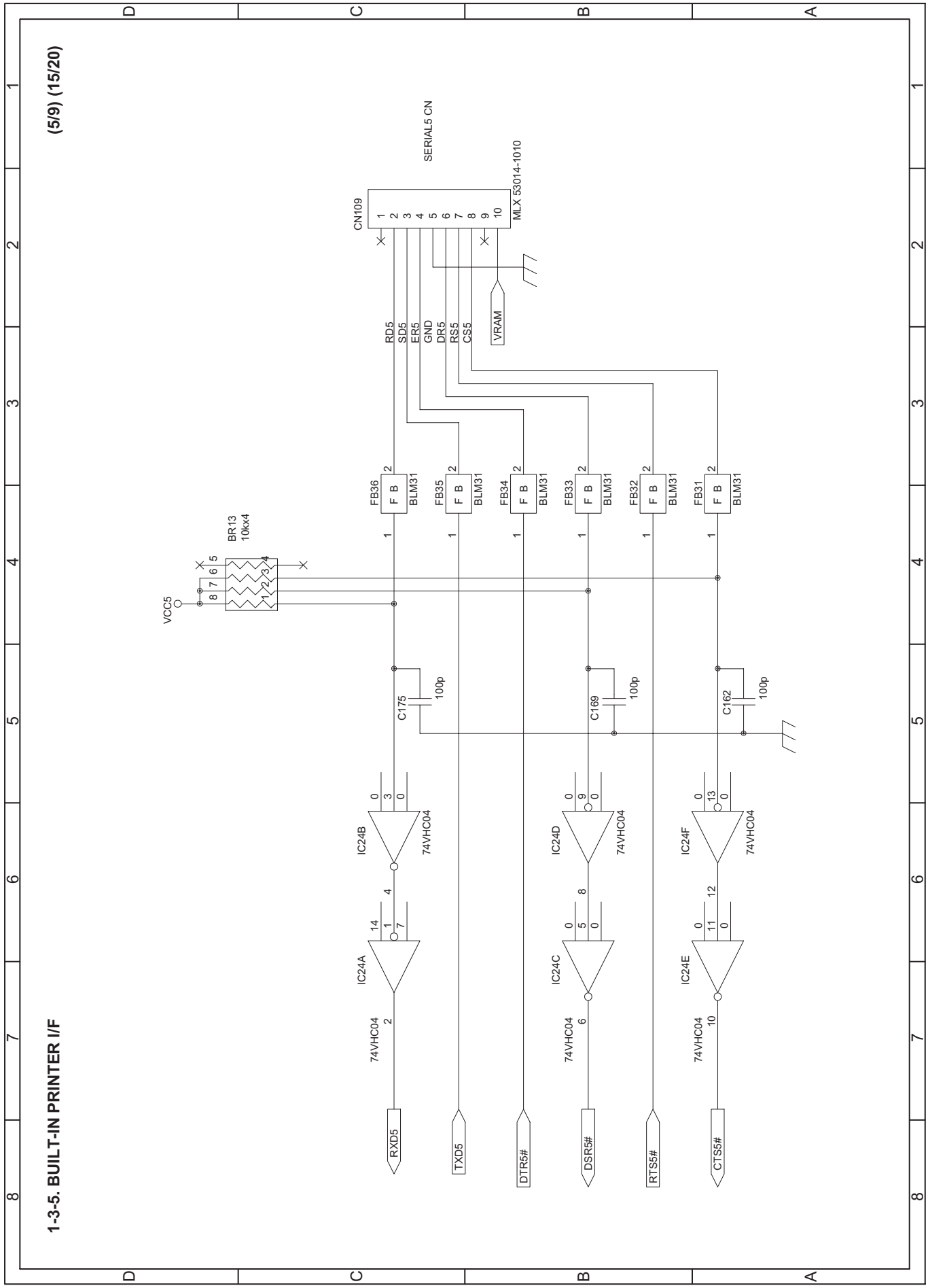


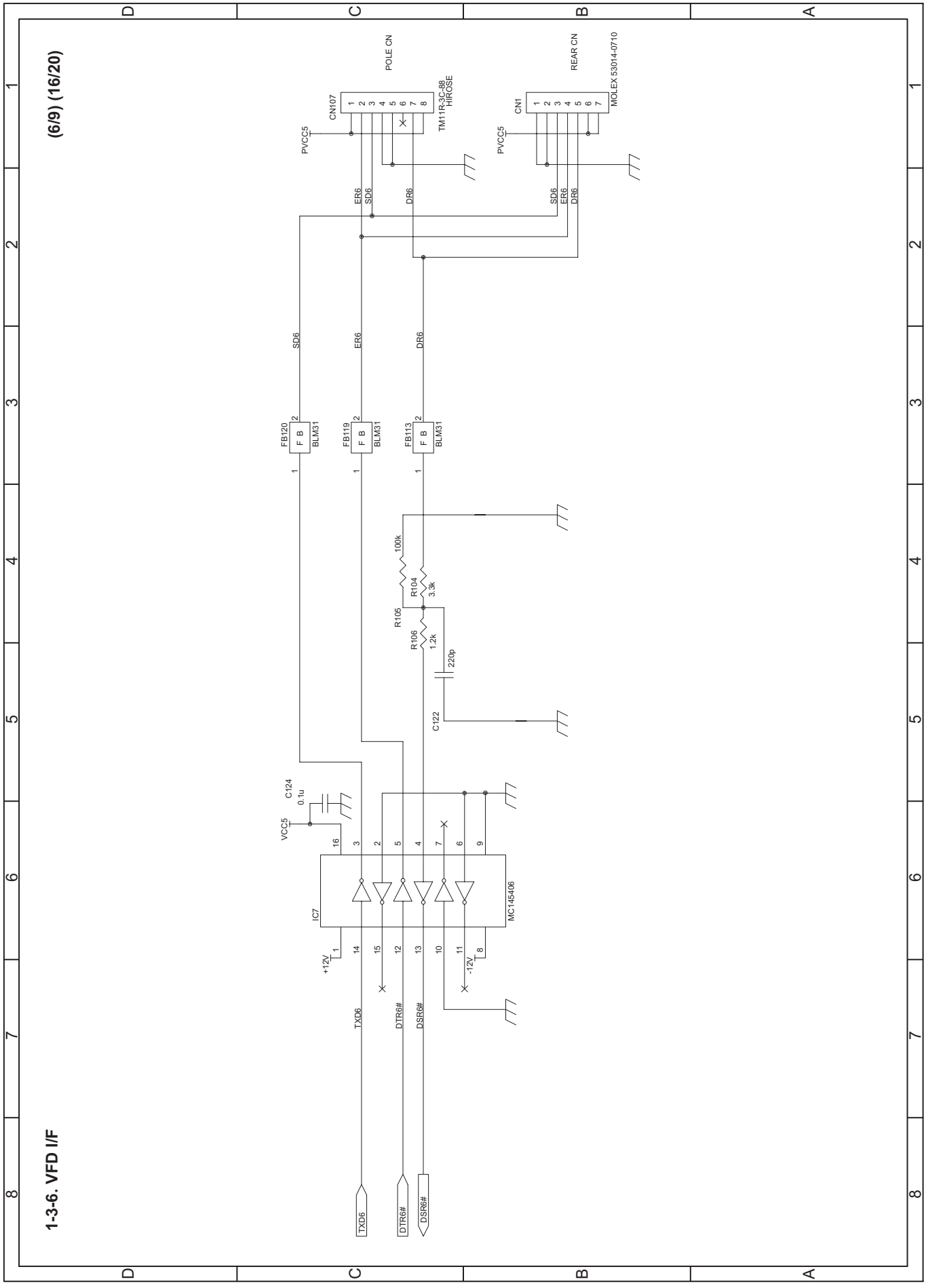
1-3-4. SERIAL 3 & 4



(5/9) (15/20)

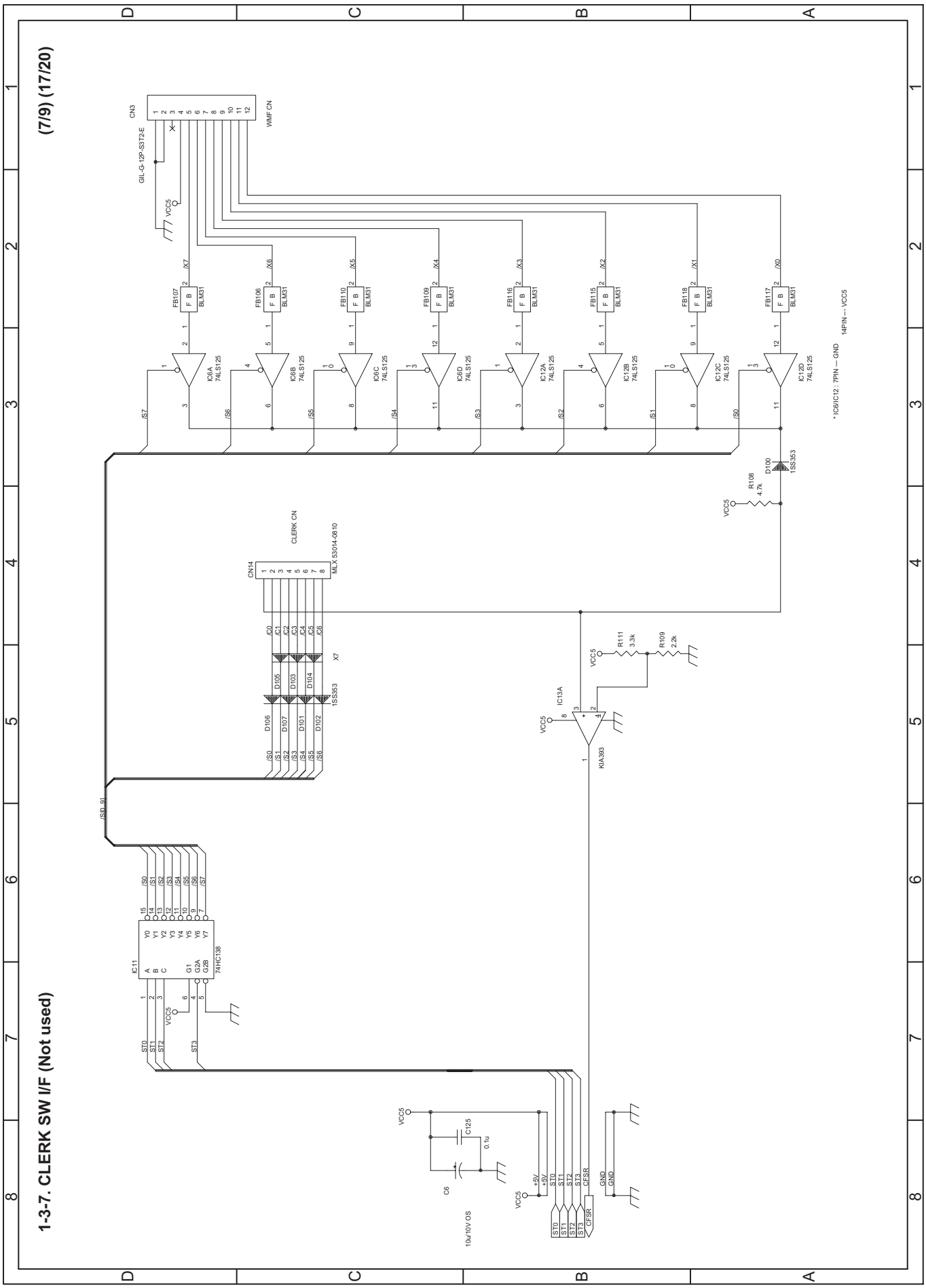
1-3-5. BUILT-IN PRINTER I/F

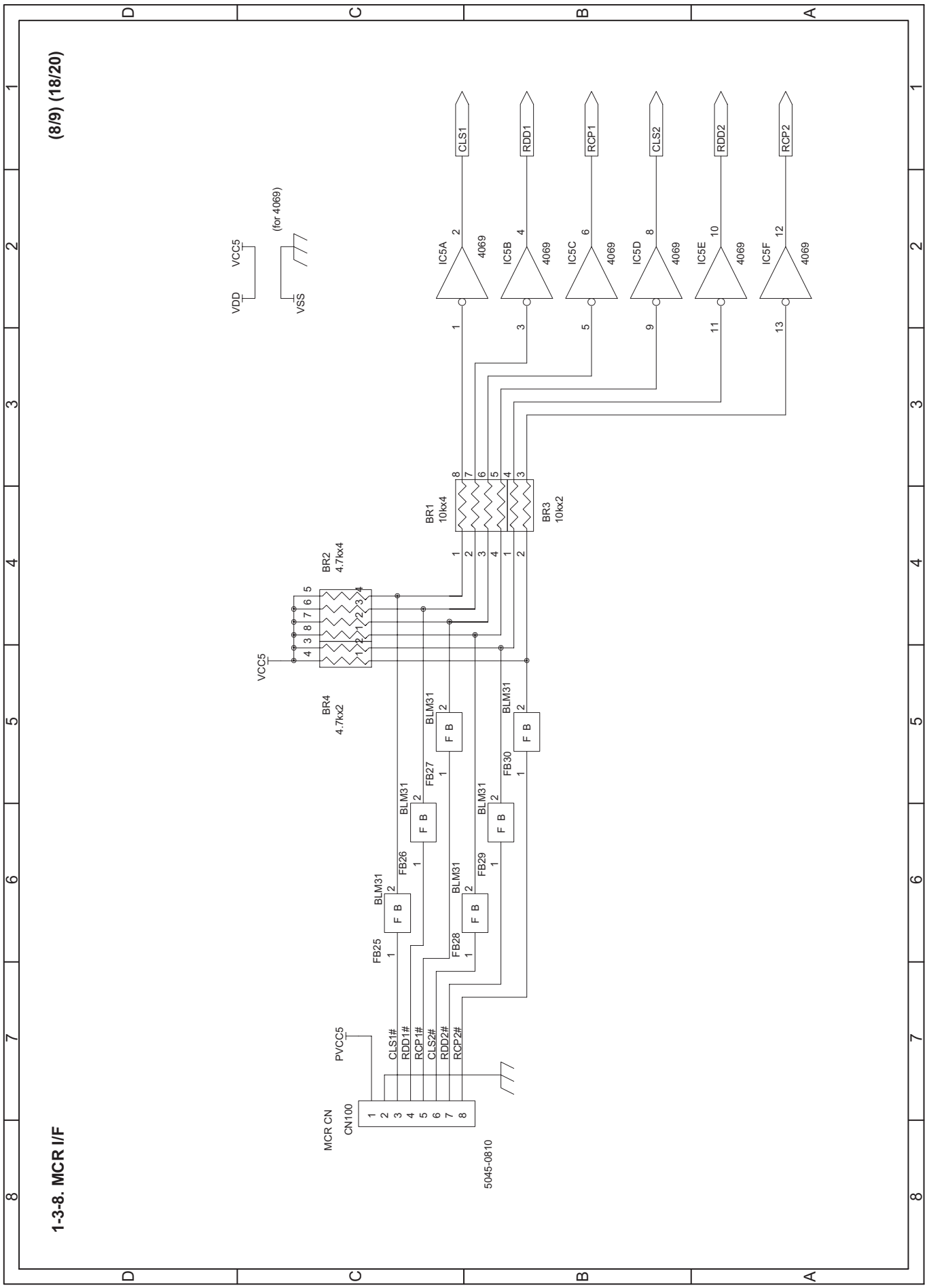


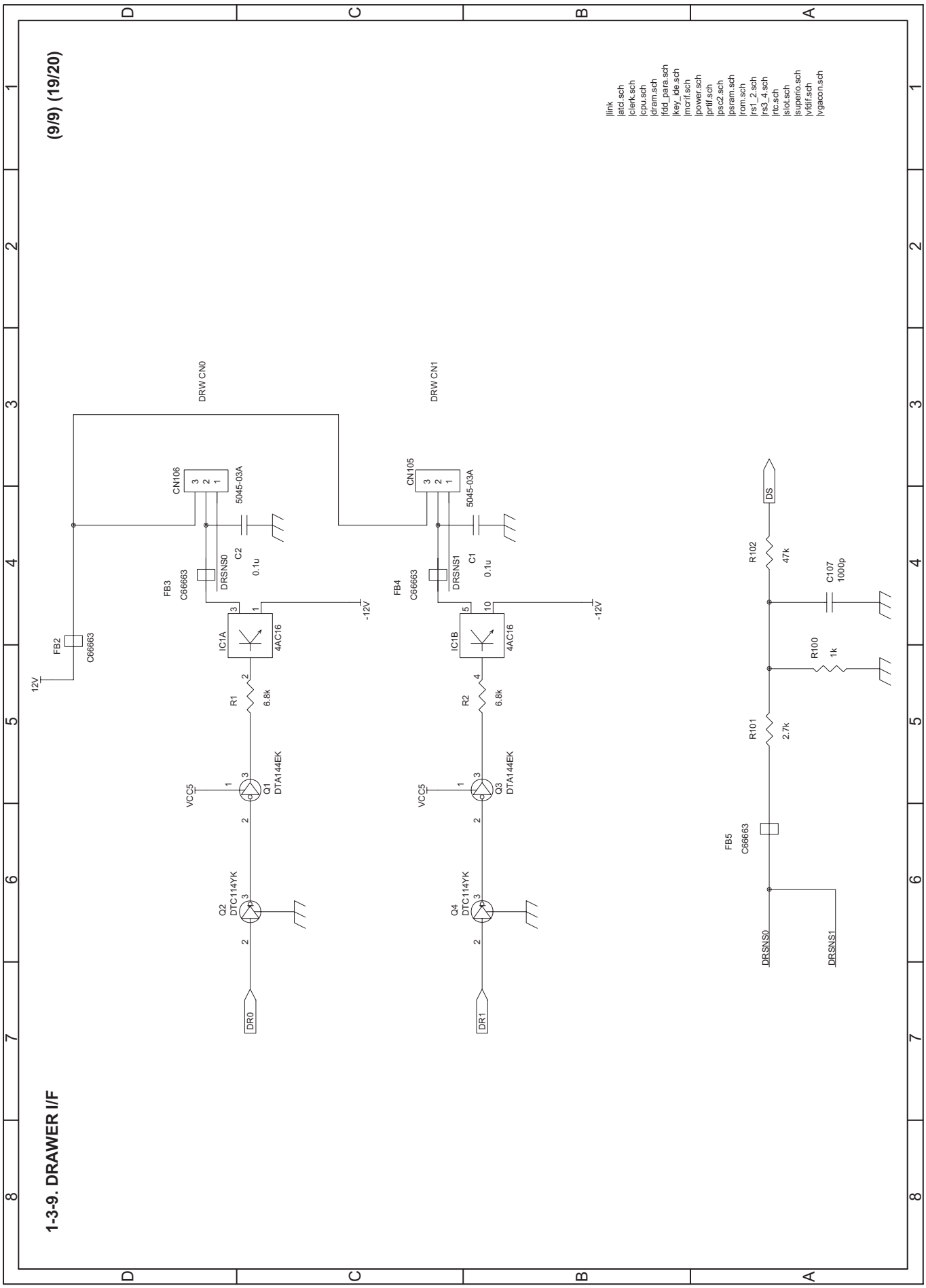

(6/9) (16/20)
1-3-6. VFD I/F
POLE CN
TM11R-3C-08
HIROSE
CN107
REAR CN
MOLEX 53014-0710
CN1
PVCC5
SD6
ER6
DR6
FB120
FB119
FB113
BLM31
100k
R104
3.3k
R105
R106
1.2k
220p
C122
C124
0.1u
VCC5
IC7
MC145406
+12V
-12V
TXD6
DTR6#
DSR6#

1-3-7. CLERK SW I/F (Not used)

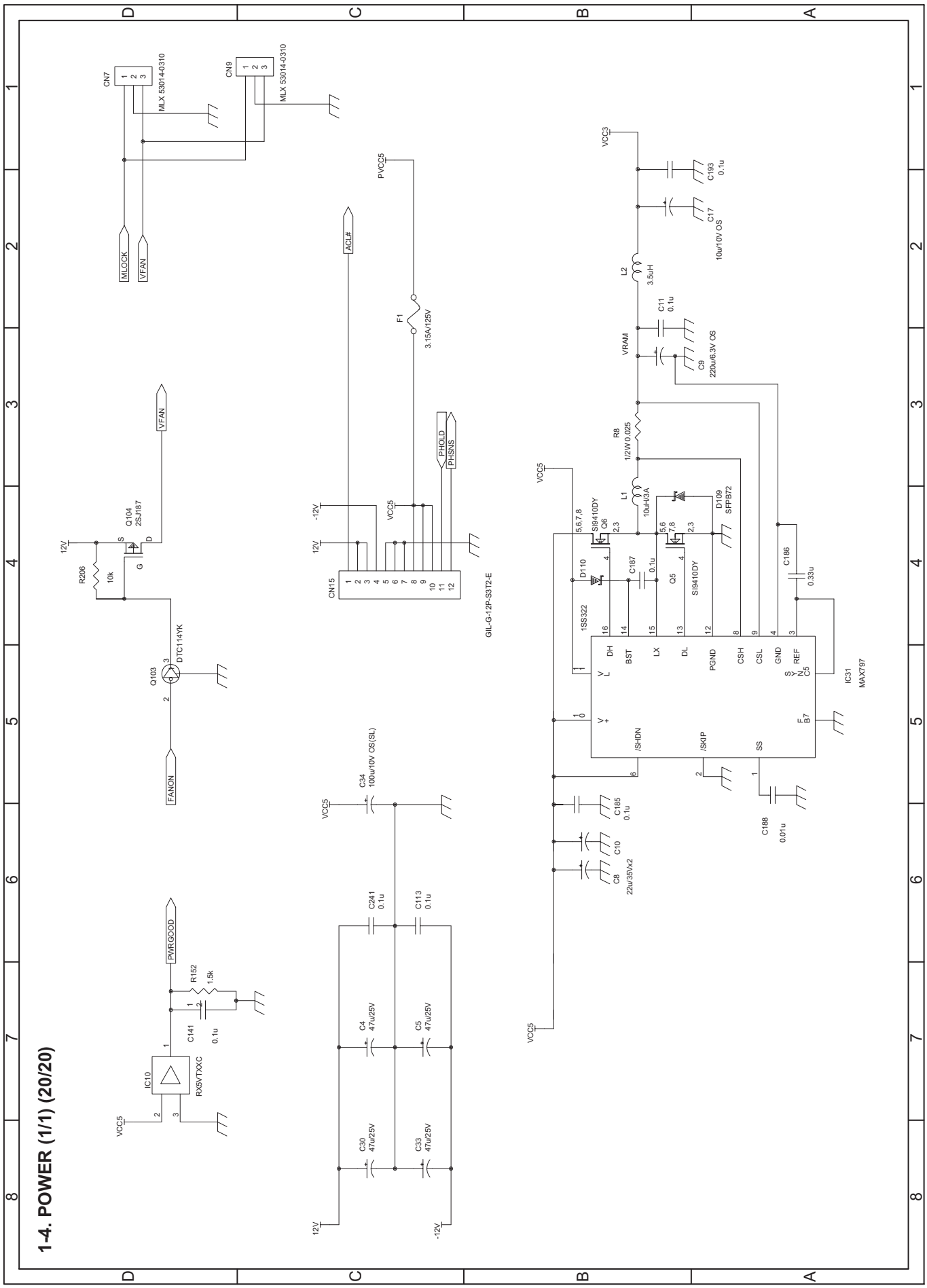
(7/9) (17/20)



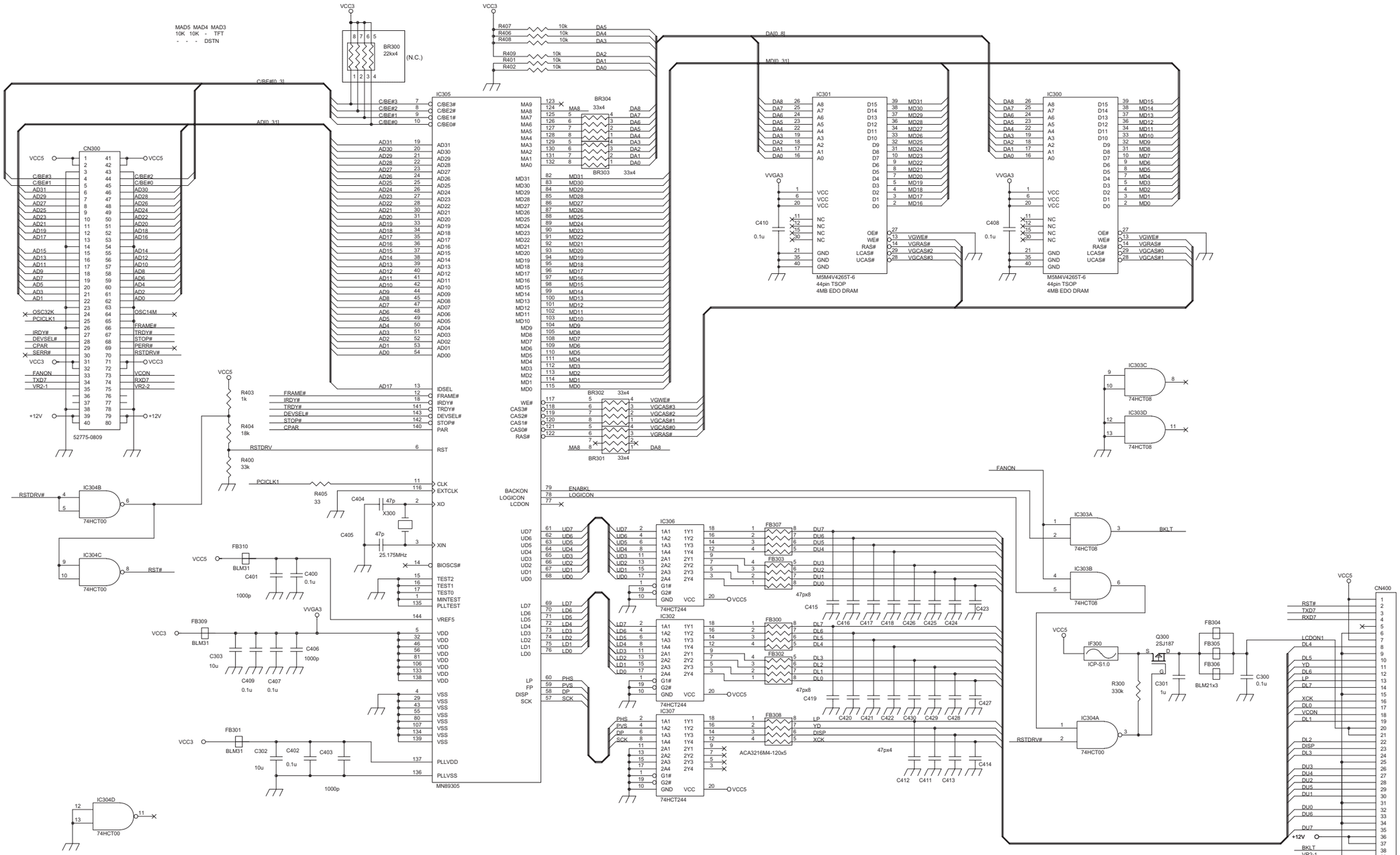

(8/9) (18/20)
1-3-8. MCR I/F
VCC5
VDD
VSS
(for 4069)
IC5A
IC5B
IC5C
IC5D
IC5E
IC5F
4069
CLS1
RDD1
RCP1
CLS2
RDD2
RCP2
BR1
10kx4
BR2
4.7kx4
BR3
10kx2
BR4
4.7kx2
BLM31
FB25
FB26
FB27
FB28
FB29
FB30
PVCC5
CLS1#
RDD1#
RCP1#
CLS2#
RDD2#
RCP2#
MCR CN
CN100
5045-0810


(9/9) (19/20)
1-3-9. DRAWER I/F
|link
|atcl.sch
|clerk.sch
|cpu.sch
|dram.sch
|fdd_para.sch
|key_ide.sch
|mcrif.sch
|power.sch
|prtif.sch
|psc2.sch
|psram.sch
|rom.sch
|rs1_2.sch
|rs3_4.sch
|rtc.sch
|slot.sch
|superio.sch
|vfdif.sch
|vgacon.sch
DRW CN0
DRW CN1
CN106
CN105
5045-03A
FB2
FB3
FB4
FB5
C66663
DRSNS0
DRSNS1
C2
C1
0.1u
12V
-12V
IC1A
IC1B
4AC16
R1
R2
6.8k
VCC5
Q1
Q3
DTA144EK
Q2
Q4
DTC114YK
DR0
DR1
DS
R102
47k
C107
1000p
R100
1k
R101
2.7k

1-4. POWER (1/1) (20/20)



2. VGA PWB (1/1)


MAD5 MAD4 MAD3
10K 10K - TFT
- - - DSTN
BR300
22kx4
(N.C.)
C/BE#[0..3]
AD[0..31]
CN300
52775-0809
IC305
MN89305
IC301
IC300
M5M4V4265T-6
44pin TSOP
4MB EDO DRAM
DA[0..8]
MD[0..31]
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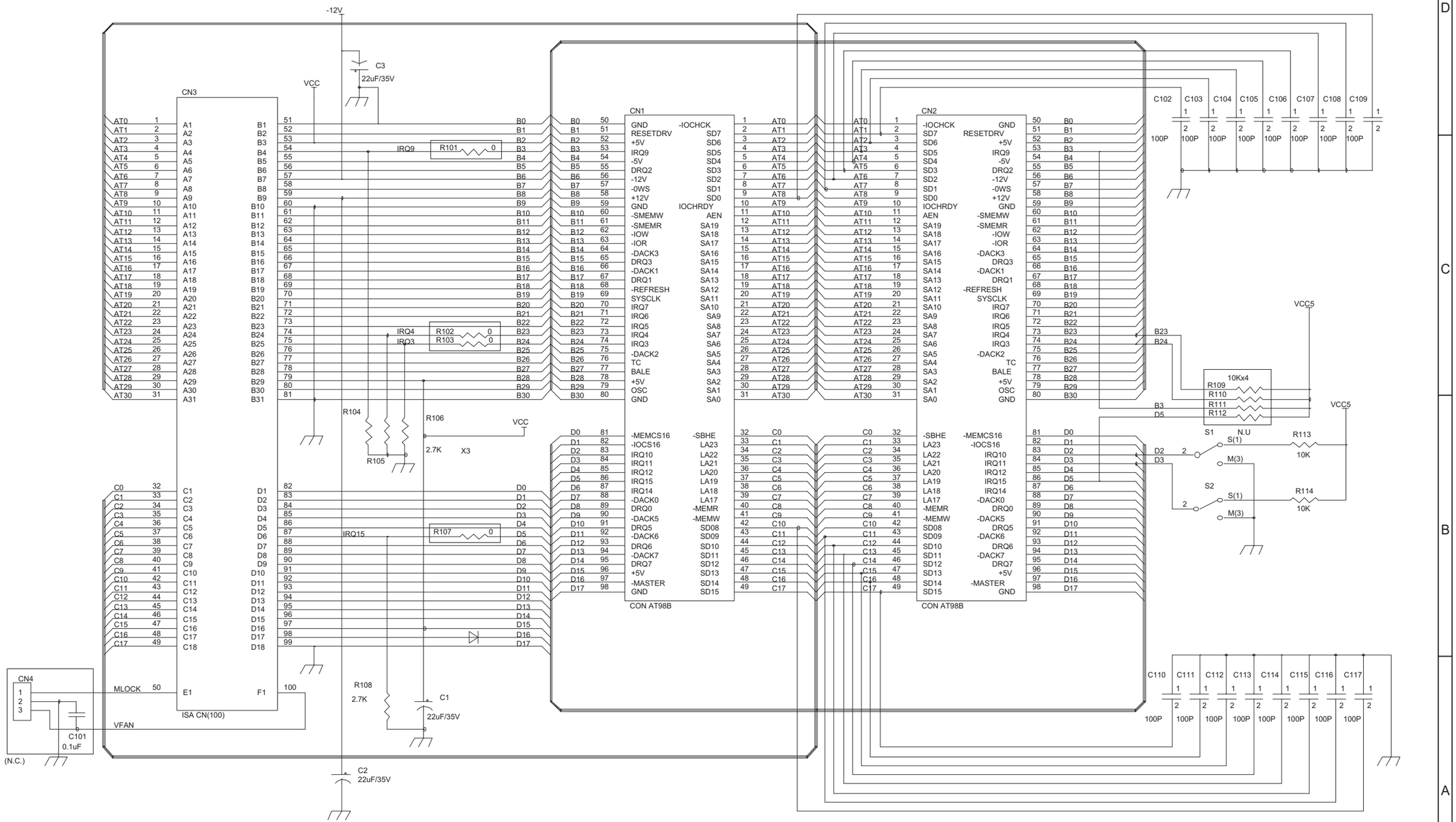
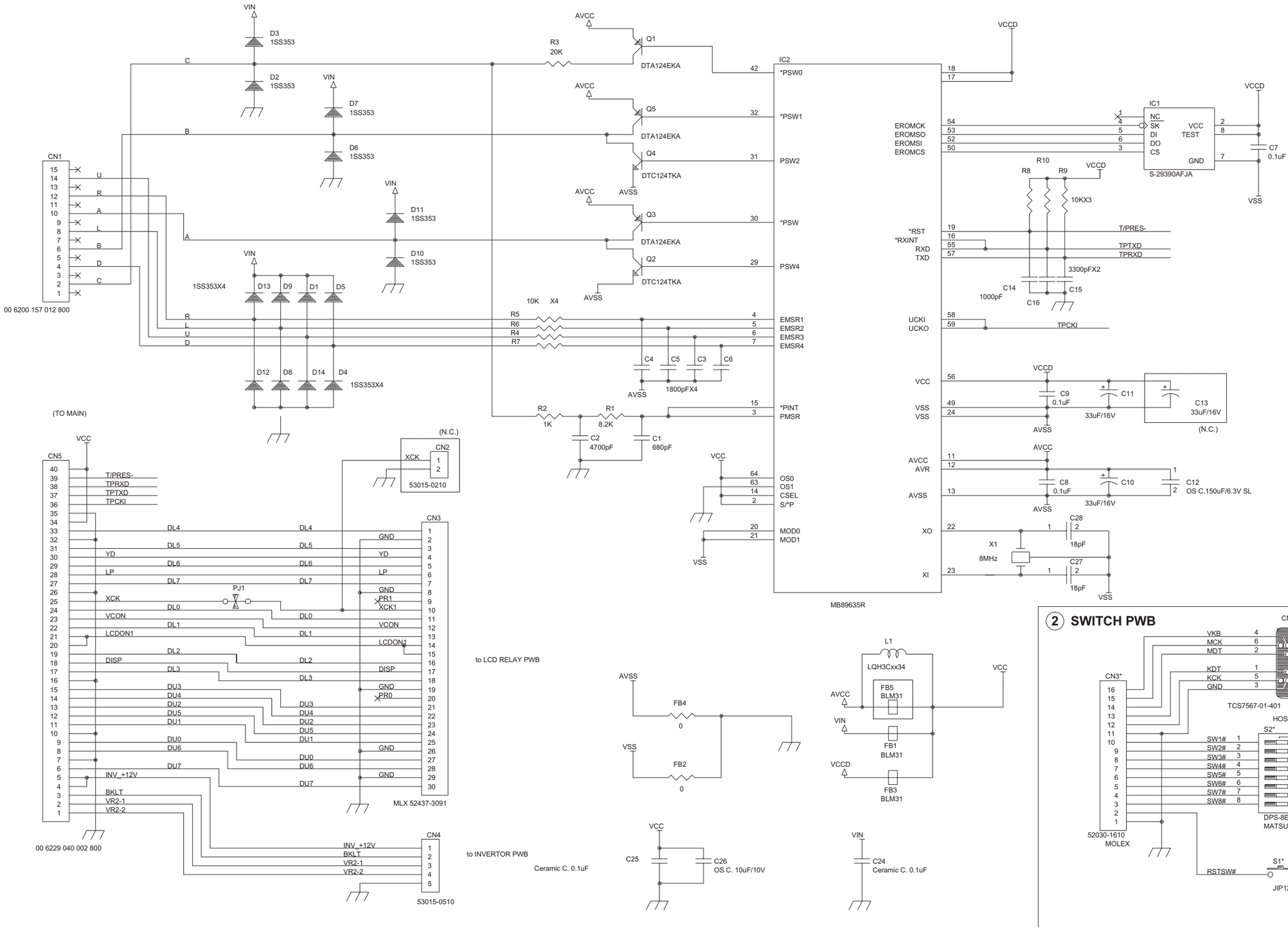
BR303
BR302
BR301
33x4
VVGA3
C410
C408
0.1u
IC306
IC302
IC307
74HCT244
FB307
FB303
FB300
FB302
FB308
47px8
47px4
ACA3216M4-120x5
IC303C
IC303D
74HCT08
IC303A
IC303B
IC304A
IC304B
IC304C
IC304D
74HCT00
FANON
BKLT
IF300
ICP-S1.0
Q300
2SJ187
R300
330k
C301
1u
FB304
FB305
FB306
BLM21x3
C300
0.1u
CN400
00 6229 640 003 800
R403
1k
R404
18k
R400
33k
R405
33
C404
47p
X300
C405
47p
25.175MHz
FB310
FB309
FB301
BLM31
C401
1000p
C400
0.1u
C303
10u
C409
0.1u
C407
0.1u
C406
1000p
C302
10u
C402
0.1u
C403
1000p
R407
R406
R408
R409
R401
R402
10k
C415
C416
C417
C418
C426
C425
C424
C423
C419
C420
C421
C422
C430
C429
C428
C427
C412
C411
C413
C414
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
CPAR
RSTDRV
PCICLK1
BACKON
LOGICON
LCDON
ENABKL
LOGICON
VGWE#
VGCAS#3
VGCAS#2
VGCAS#1
VGCAS#0
VGRAS#
VGRAS#
VGCAS#2
VGCAS#3
VGCAS#0
VGCAS#1

3. RISER PWB (1/1)

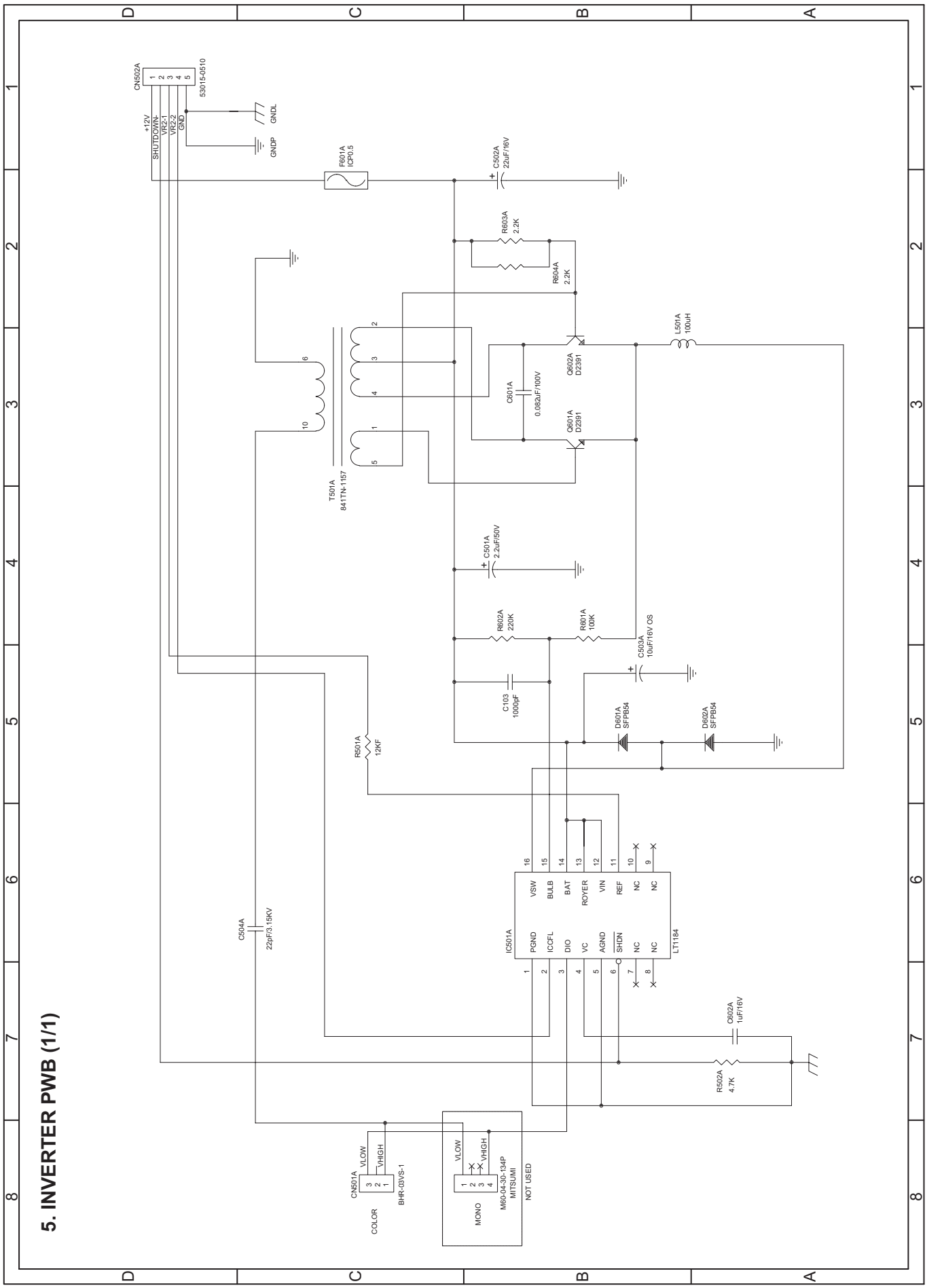


4. TOUCH PANEL CONTROL PWB (1/1) & SWITCH PWB (1/1)

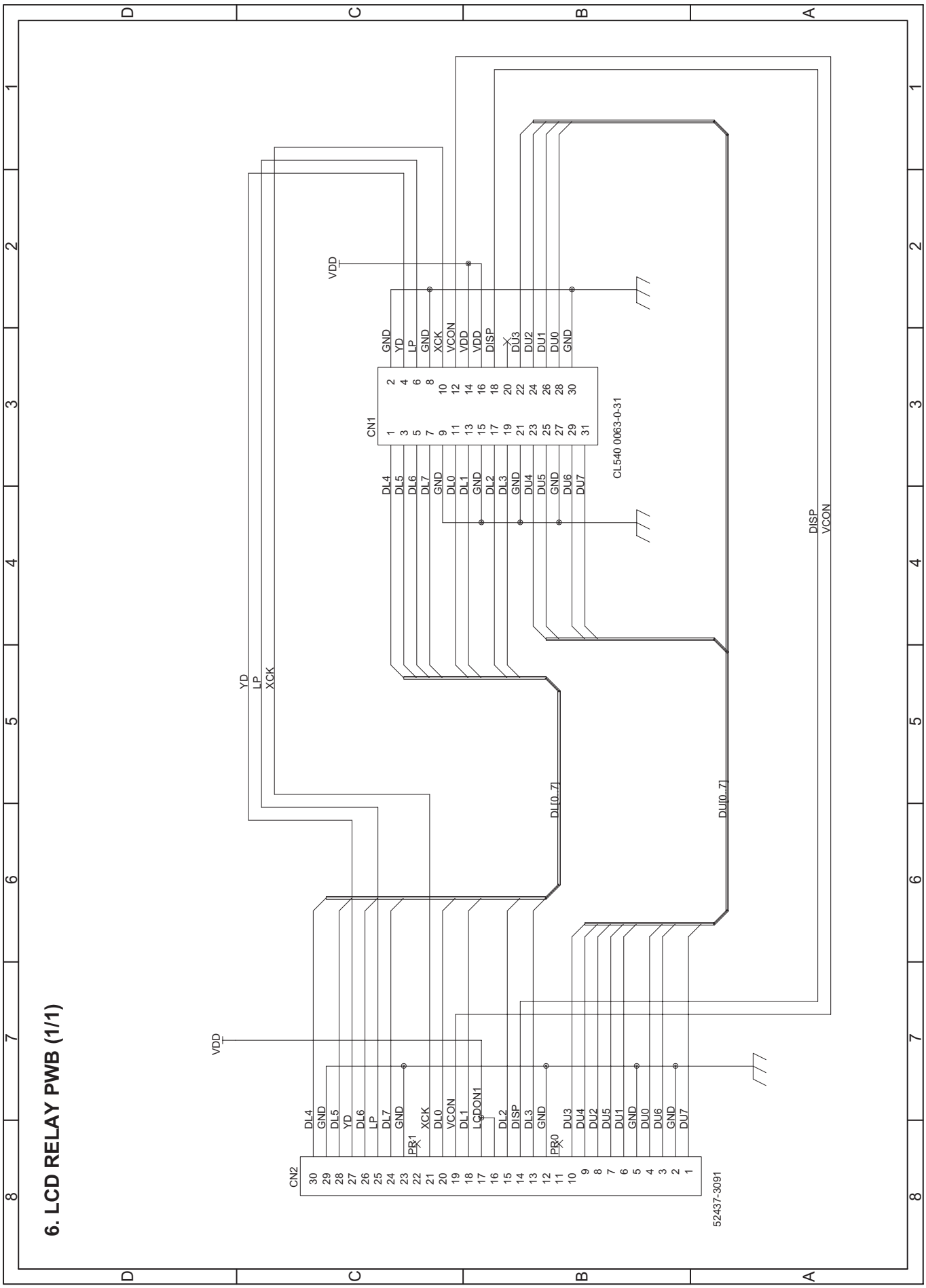
(1) TOUCH PANEL CONTROL PWB



5. INVERTER PWB (1/1)



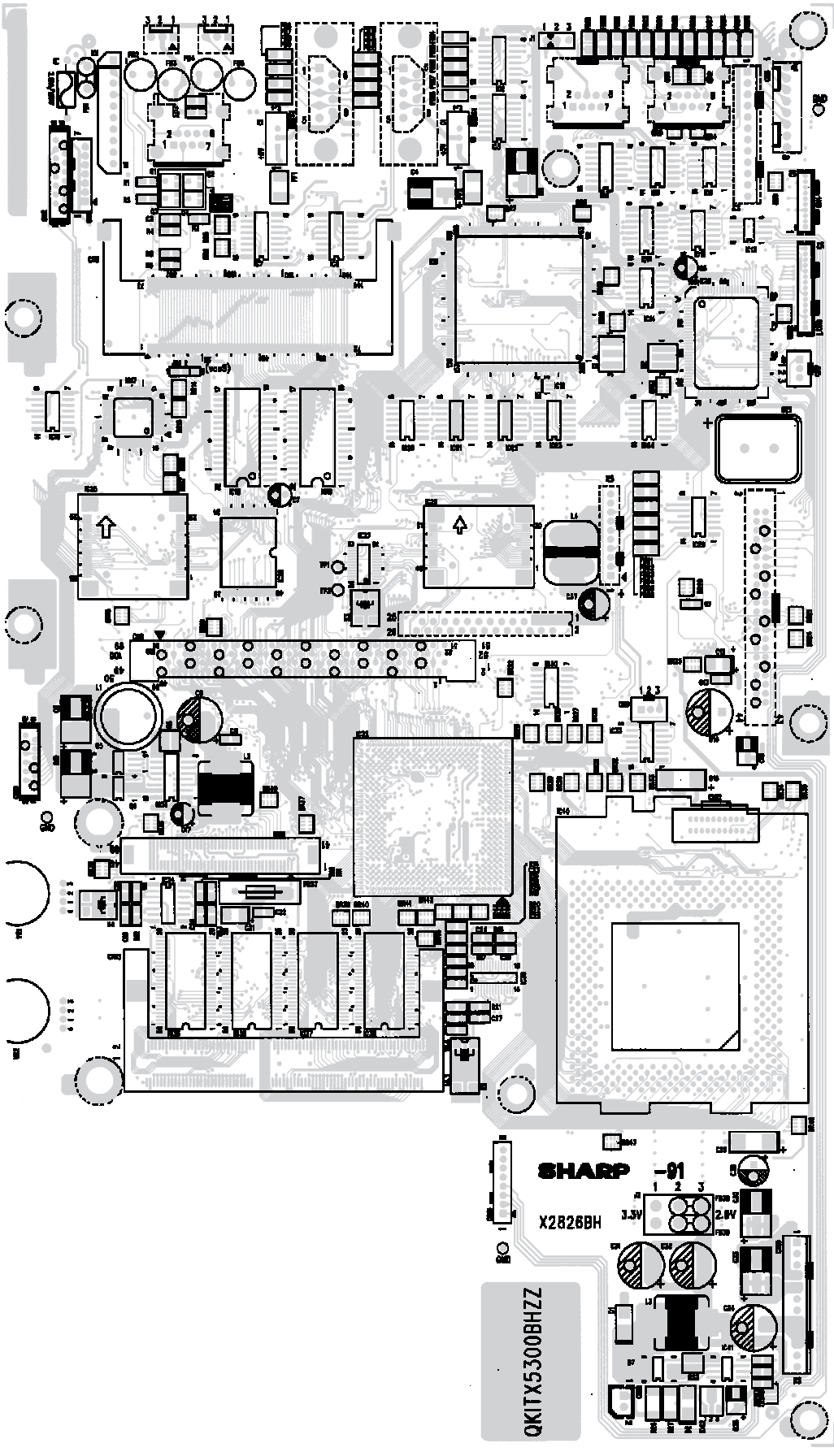
6. LCD RELAY PWB (1/1)



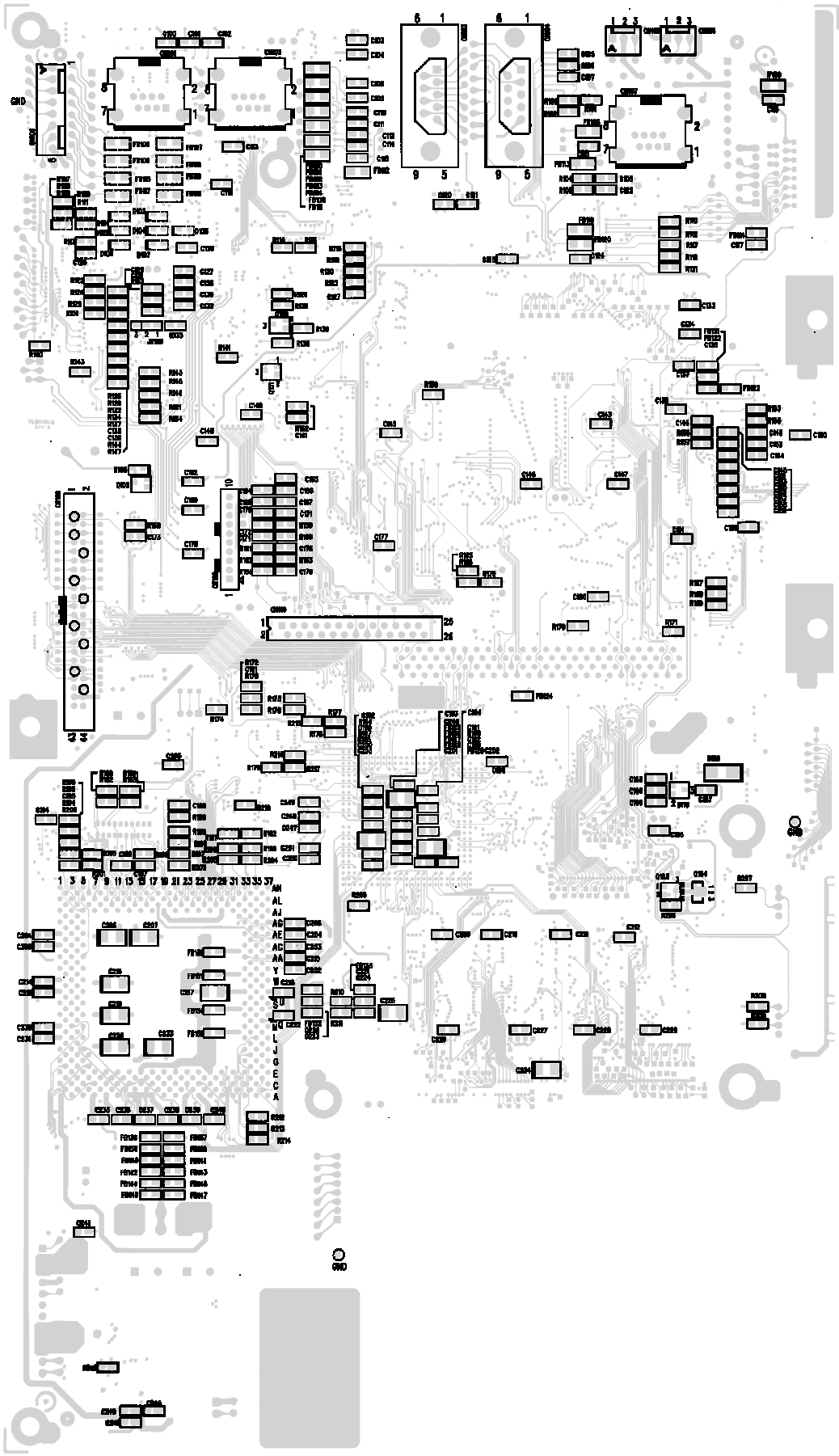
CHAPTER 9. PWB LAYOUT

1. Main PWB

[A Side]

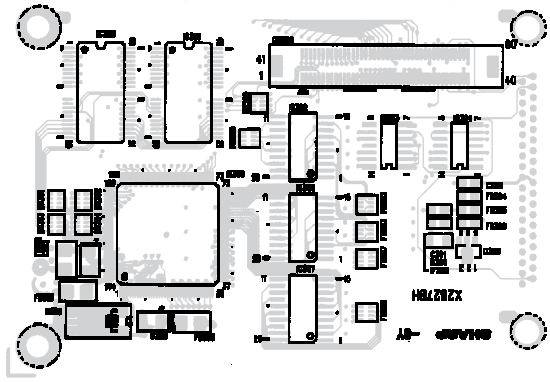


[B Side]

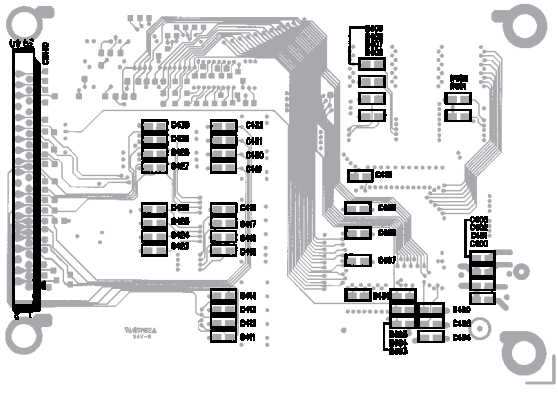


2. VGA PWB

[A Side]

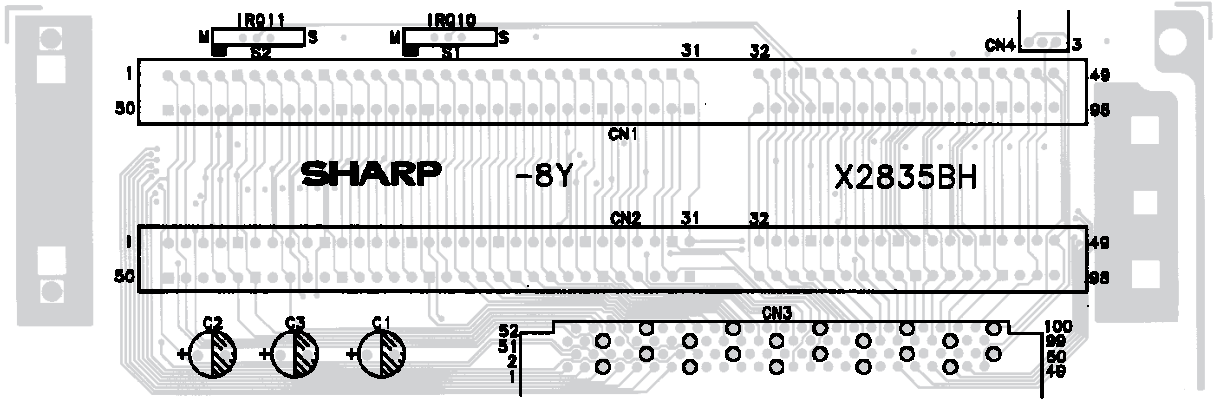


[B Side]

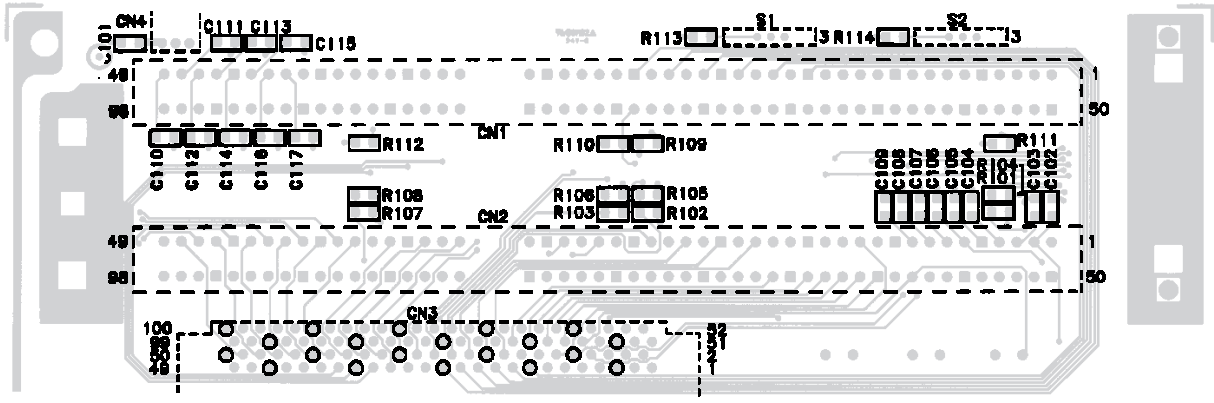


3. Riser PWB

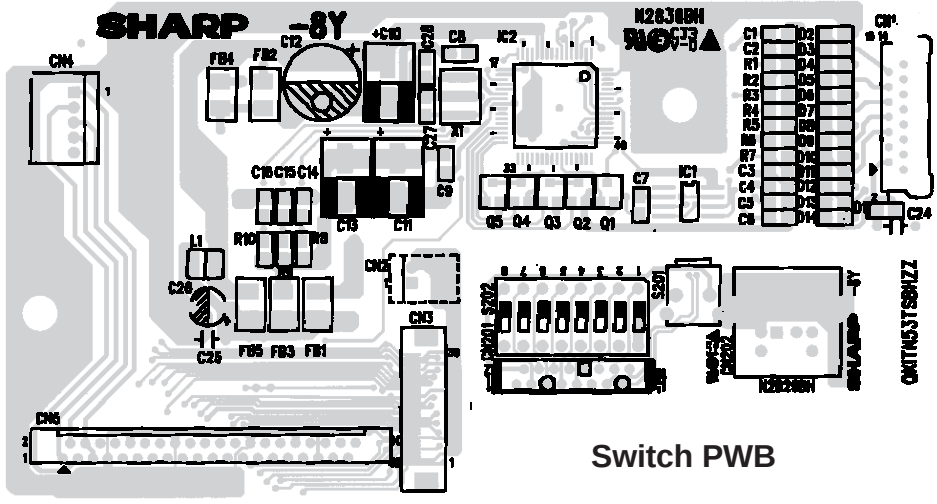
[A Side]



[B Side]

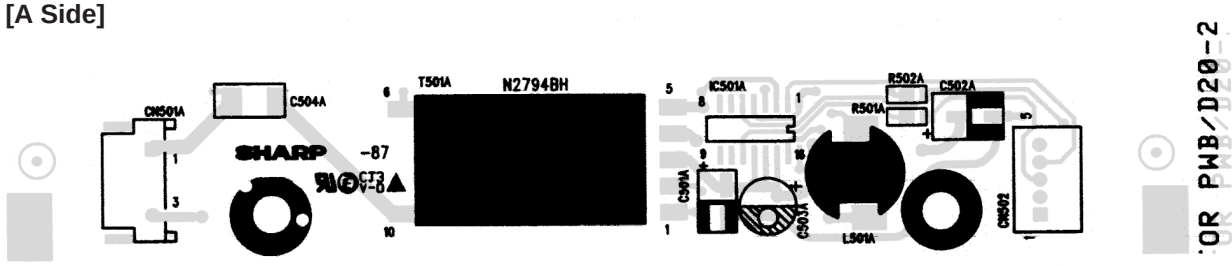


4. T/P Switch PWB

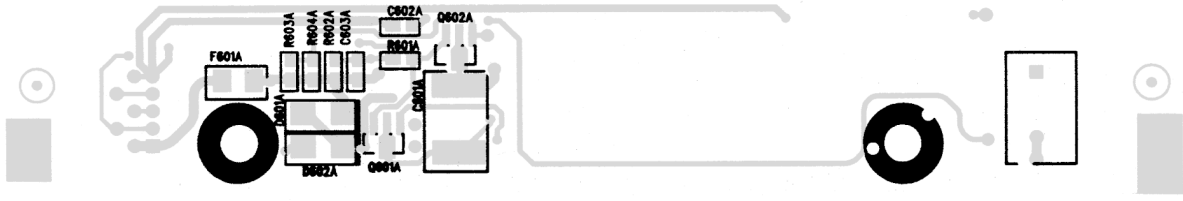


5. INVERTER PWB

[A Side]

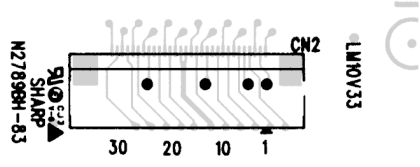


[B Side]

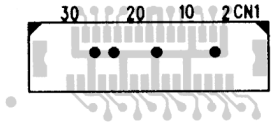


6. LCD RELAY PWB

[A Side]



[B Side]



UP-5300V

SHARP PARTS GUIDE

MODEL UP-5300

(for KB,TQ,TS)

CONTENTS

1 Top cabinet etc.
2 Bottom cabinet etc.
3 Packing material & Accessories
4 Main PWB unit
5 VGA PWB unit
6 Touch panel PWB unit
7 Inverter PWB unit
8 Riser PWB unit
9 SW PWB unit
10 LCD PWB unit
11 Service route options & Service tools
■ Index

Because parts marked with "⚠" is indispensable for the machine safety maintenance and poeration, it must be replaced with the parts specific to the product specification.

Table of destinations

SELECTION CODE	COUNTRIES
U	U.S.A., Guam
A	Canada
TS	Germany
TQ	SEEG territory other than Germany (Stamp:English)
TR	SEEG territory other than Germany (Stamp:English)
KB	U.Kingdom
KA	Australia

SELECTION CODE	COUNTRIES
K	Korea

SELECTION CODE	COUNTRIES
SB	Saudi Arabia (127V area)
SBA	Saudi Arabia (220V area)
SC	Taiwan
SD	Venezuela
SE	Hong Kong
SG	Lebanon, Syria, Greece, Pakistan, Iran, Egypt, Thailand, Iraq, Mauritius, Seychelles, Tahiti, Jordan, Sudan, Turkey
SH	South Africa (U.S.A. version)
SHE	South Africa (Europe version)
SJ	Philippines (Europe version)
SJ2	Philippines (U.S.A. version)
SM	Kuwait, Qatar, Oman, UAE, Malta, Bahrain
SMT	Nigeria, Yemen, Kenya

SELECTION CODE	COUNTRIES
RA1	Morocco, Algeria, Tunisia, West Africa
RA2	Chile, Uruguay, Peru, Argentina, Paraguay
RA5	Sri Lanka

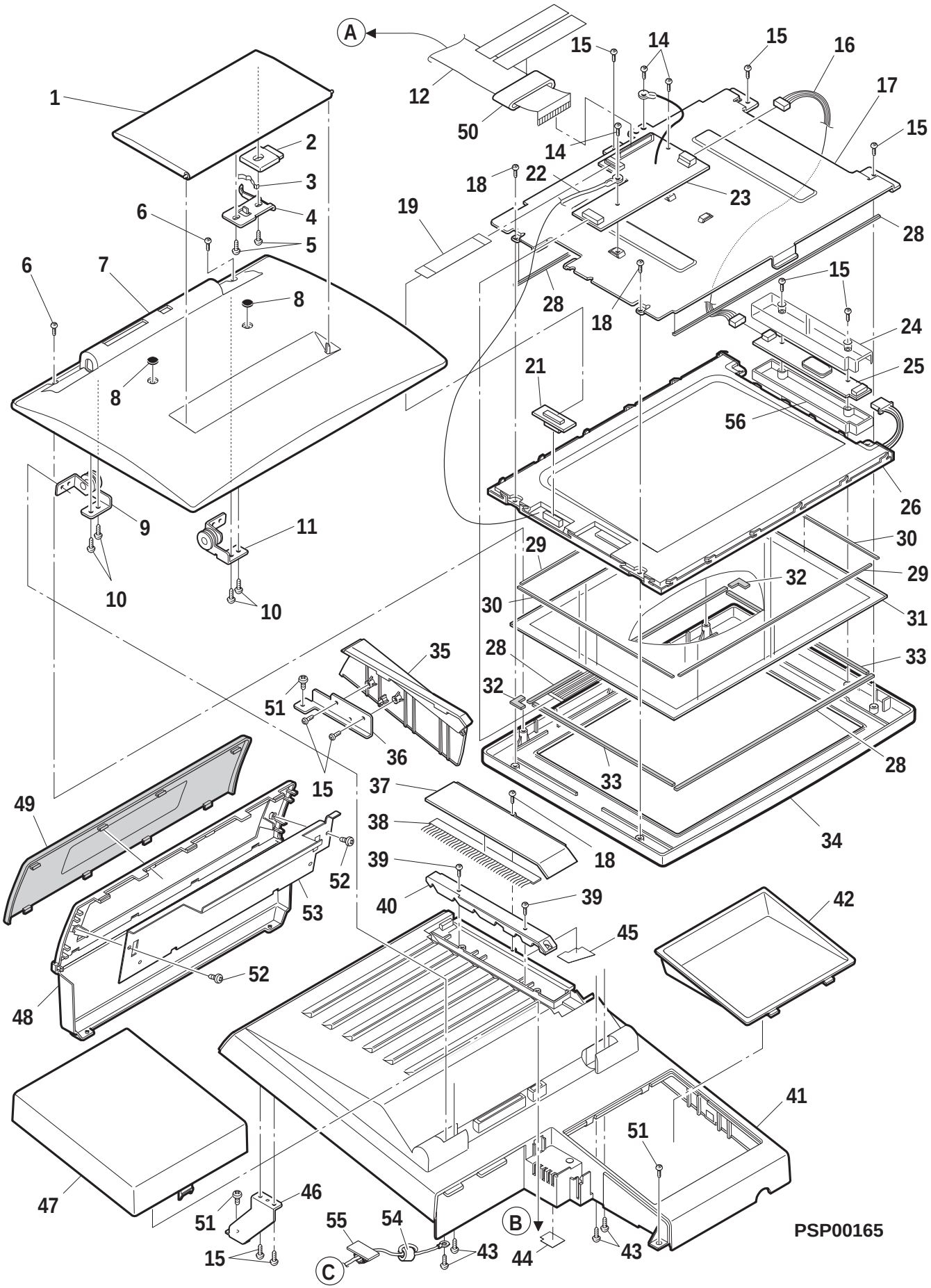
SELECTION CODE	COUNTRIES
RB3	Indonesia
RB4	
RB5	Cyprus
RB6	Panama
RB7	Barbados
RB8	Malaysia (U.S.A. version)

SELECTION CODE	COUNTRIES
RC1	Malaysia (Europe version)
RC2	Singapore
RC5	Dominican Republic, Ecuador

1 Top cabinet etc.

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	GSTN-2005BHZZ	AT		C	Tilt stand
2	JKNBZ2411BHZZ	AH		C	Tilt knob
3	MSPRP2372BHZZ	AE		C	Tilt spring
4	MLEVF2324BHZZ	AG		C	Tilt lever
5	LX-BZ6787BHZZ	AB		C	Screw (3×5)
6	XJSSD30P10000	AA		C	Screw (3×10)
7	GCABF7873BHSA	BP		D	LCD rear cabinet
8	PGUMM2389BHZZ	AE		C	LCD cushion
9	MHNG-2324BHZZ	AX		C	Hinge L
10	XUBSD40P08000	AA		C	Screw (4×8)
11	MHNG-2325BHZZ	AX		C	Hinge R
12	QCNW-2972BHZA	AR		C	Flat cable (40P)
14	XHBSD30P05000	AA		C	Screw (3×5)
15	XEBSD30P08000	AA		C	Screw (3×8)
16	QCNW-2976BHZZ	AK		C	Inverter cable
17	LANGK7649BHZZ	AV		C	LCD plate
18	XEPSD30P08000	AA		C	Screw (3×8)
19	QCNW-2973BHZZ	AS		C	Flat cable (30P 0.5mm PITCH)
21	CPWBN2789BH02	AY		E	LCD PWB unit
22	QCNW-2996BHZZ	AD		C	LCD GND wire
23	CPWBN2836BH01	BR		E	Touch panel PWB unit
24	GCŌVH7167BHZZ	AH		D	Invertor cover
25	CPWBN2794BH01	BQ		E	Inverter PWB unit
26	VVLLM10V33/-1	CS		B	LCD (LM10V33)
28	PGUMM6731BHZZ	AR		C	T/P gum B
29	PGUMM6733BHZZ	AR		C	LCD gum B
30	PGUMM6732BHZZ	AS		C	LCD gum A
31	HPNLC6839RCZZ	BT		D	Touch panel
32	PGUMM6734BHZZ	AL		C	T/P gum C
33	PGUMM6730BHZZ	AS		C	T/P gum A
34	GCABE7872BHSA	BL		D	LCD front cabinet
35	GCŌVA7159BHSA	BD		D	Side cover
36	LANGK7651BHZZ	AL		C	Cab angle 2
37	GCŌVA7166BHZZ	AP		D	Tilt cover
38	PSHEG2859BHZZ	AV		C	Dust sheet
39	XJSSD30P08000	AA		C	Screw (3×8)
40	JKNBZ6923BHZZ	AP		C	Tilt lock
41	GCABB7870BHSA	BV		D	Top cabinet
42	GFTAT6927BHZB	BD		D	Keyboard lid
43	XBBSD30P08000	AA		C	Screw (3×8)
44	PSHEP2472BHZZ	AH		C	W sheet 2
45	PSHEP2471BHZZ	AH		C	W sheet 1
46	LANGK7650BHZZ	AH		C	Cab angle 1
47	GFTAT6928BHZZ	AV		D	Printer lid
48	GCŌVA7158BHSA	BG		D	Rear cover
49	PFiLW6979BHZA	AX		D	Rear filter
50	RCŌRF2031SCZZ	AN		C	Core (SSC-50-12-F)
51	XUBSD40P12000	AA		C	Screw (4×12)
52	XEBSD30P06000	AA		C	Screw (3×6)
53	LANGT2847BHZZ	AP		C	R cover angle
54	RCŌRF6712BHZZ	AG		C	Core (OP14C)(RCORFOP14CHZZ)
55	LHLDW6821BHZZ	AD		C	Q-clamp (S)
56	PSHEP2874BHZZ	AH		C	Invertor sheet

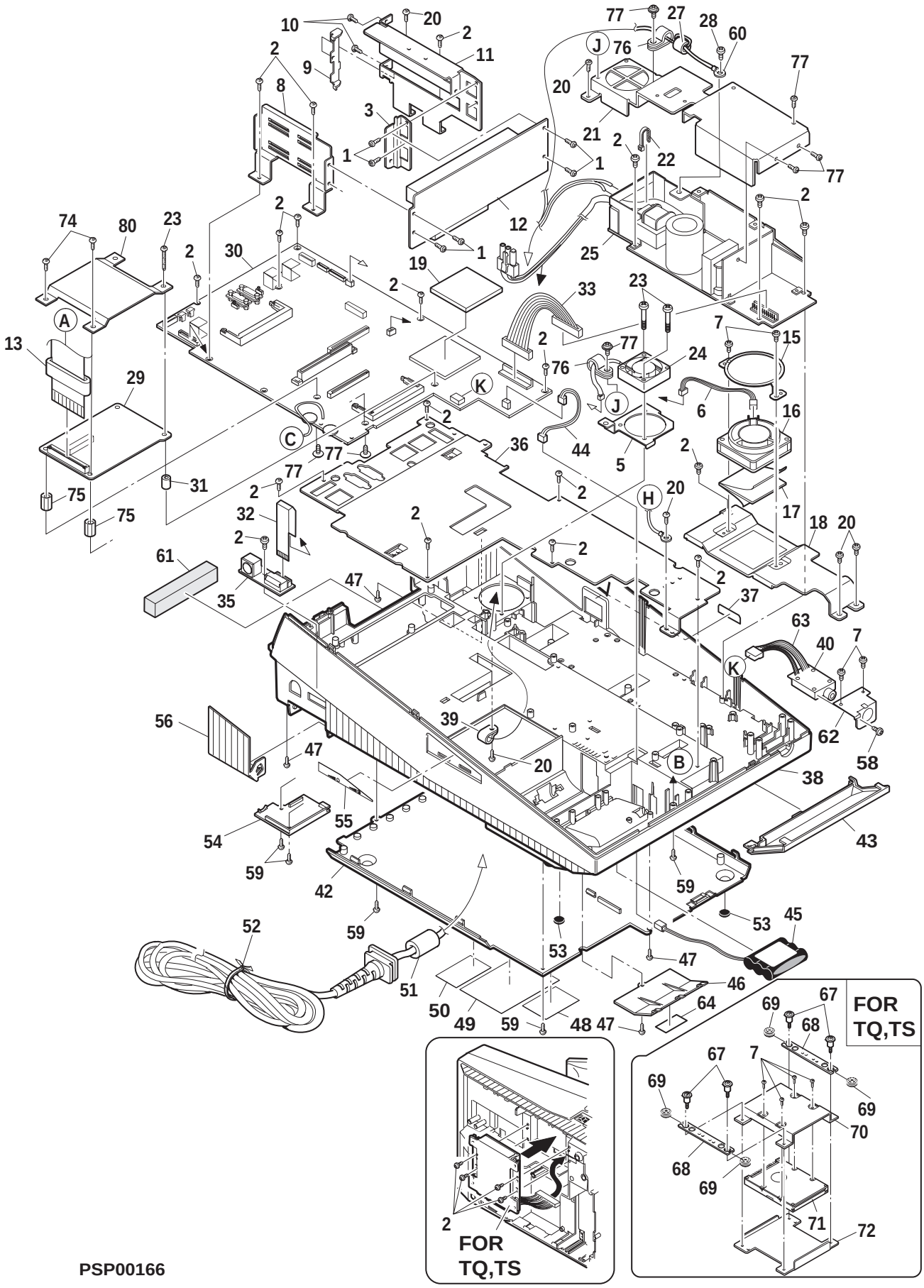
1 Top cabinet etc.



2 Bottom cabinet etc.

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	LX-BZ6782BHZZ	AA		C	Screw
2	XEBSD30P08000	AA		C	Screw (3×8)
3	LANGK2839BHZZ	AR		C	Option angle 3
5	LPLTM6723BHZZ	AT		C	Fan plate
6	QCNW-7864BHZZ	AG		C	CPU fan cable
7	XBBSD30P04000	AA		C	Screw (3×4)
8	LANGT7638BHZZ	AM		C	Option angle 2
9	LANGT2808BHZZ	AK		C	Option angle 4
10	LX-BZ6778BHZZ	AA		C	Screw (3×6)
11	LANGT7637BHZZ	AT		C	Option angle 1
12	CPWBX2835BH01	BQ		E	Riser PWB unit
13	RCŌRF2031SCZZ	AN		C	Core (SSC-50-12-F)
15	MSPRE6756BHZZ	AQ		C	FAN spring
16	NFANP6003RCZZ	BF		B	CPU cooler fan
17	PSHEP6859BHZZ	AN		C	CPU sheet
18	PRDAF2350BHZZ	AR		C	CPU heat sink
19	PSHEG6863RCZZ	AR		C	CPU gum
20	XHBSD30P06000	AA		C	Screw (3×6)
21	GCŌVH7168BHZZ	AZ		D	PS cover
22	LBNDJ2003SCZZ	AA		C	Cable band (PLT1M)
23	XEBSD30P20000	AA		C	Screw (M3×20)
24	NFANP6004RCZZ	BA		B	Set u fan
25	RDENC1014RCZZ	BX	N	E	Power supply unit
27	RCŌRF6712BHZZ	AG		C	Core (OP14C)(RCORFOP14CHZZ)
28	XBPBZ40P06K00	AA		C	Screw (M4×6K)
29	CPWBX2827BH02	CF	N	E	VGA PWB unit
30	CPWBX2826BH03	DT	N	E	Main PWB unit
31	PSPAZ2380BHZZ	AD		C	VGA spacer 2
32	QCNW-3012BHZZ	AL		C	Flat cable (16P)
33	QCNW-7863BHZZ	AT		C	Power cable
35	CPWBN2829BH01	BA		E	Switch PWB unit
36	LCHSM6709BHZA	AY		C	Main chassis
37	TLABH2476BHZZ	AE		D	PS label
38	GCABA7871BHSA	BV		D	Bottom cabinet
39	LHLDW0006SCZZ	AB		C	Cable holder (3N)
40	LKGiW7375BHZA	BH		B	Clerk switch(body)
42	GCŌVH2472BHZZ	BA		D	Bottom cover
43	GFTAU2426BHZZ	AR		D	FDD lid
44	QCNW-7708BHZZ	AM		C	Battery cable (2pin)
45	UBATN2338RCZZ	BE		B	Battery (3HR-AAC)
46	GCŌVH7160BHZZ	AN		D	Battery cover
47	XJBSF30P10000	AA	N	C	Screw
48	TLABG6967BHZZ	AC		D	Battery label
49	TLABG7097BHZZ	AF		D	Battery caution label
50	TCAUS6677BHZZ	AD		D	Caution label
51	RCŌRF6695BHZZ	AK		C	Core (CP14A)
⚠	QACCV6422BHZZ	AY		B	AC cord [TQ,TS]
⚠ 52	QCNW-3061RCZZ	AS	N	B	AC cord [KB]
⚠	QPLGA0006QCZZ	AQ		C	Plug (3A 250V) [KB]
53	GLEGG6659BHZZ	AE		D	T/gum leg
54	LHLDK6847BHZZ	AN		C	AC cord cover
55	TLABH2460BHZZ	AE		D	Volume label
56	GCŌVH7161BHZZ	AN		D	AT cover
58	XJSSD26P08000	AA		C	Screw (2.6×8)
59	XEBSD30P10000	AA		C	Screw (3×10)
60	QTANP0004BHZA	AE		C	Earth terminal
61	PCUSS2404BHZZ	AG	N	C	Rear cushion
62	LANGK7657BHZZ	AK		C	Clerk angle
63	QCNW-3056BHZZ	AN	N	C	Clerk cable
64	TLABH6996BHZZ	AD		D	Battery cover seal [KB]
67	LX-BZ6794BHZZ	AE		C	Screw (M3×14) [TQ,TS]
68	LANGK7620BHZZ	AE		C	HDD plate [TQ,TS]
69	PCUSG7080RCZZ	AH		C	HDD cushion [TQ,TS]
70	GCŌVH7138BHZZ	AL		D	HDD cover A [TQ,TS]
72	GCŌVH7139BHZZ	AN		D	HDD cover B [TQ,TS]
74	XBBSD30P06000	AA		C	Screw (3×6)
75	PSPAG2379BHZZ	AH		C	VGA spacer
76	LBNDJ0007UCZZ	AB		C	Cable holder (HP-10N)
77	XBPSD30P08KS0	AA		C	Screw (3×8KS)
80	LPLTM2357BHZZ	AK		C	VGA sh plate

2 Bottom cabinet etc.

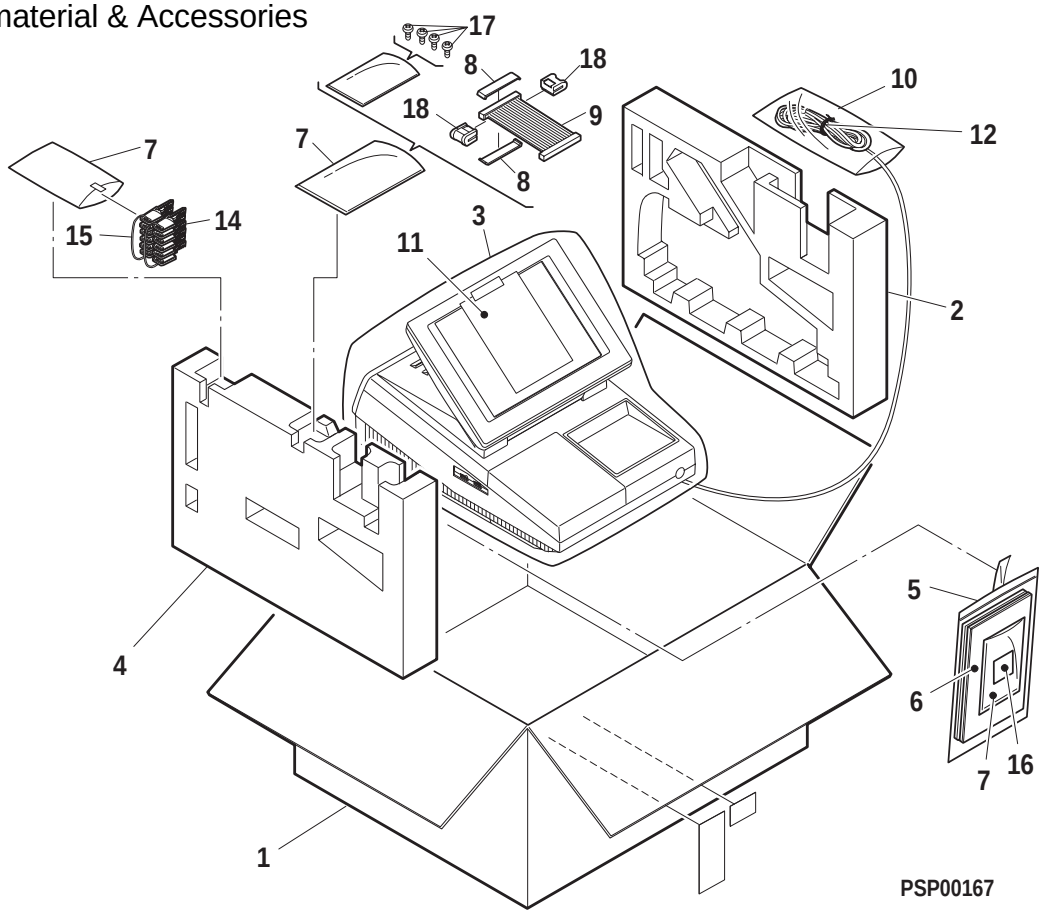


PSP00166

3 Packing material & Accessories

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	SPAKC3049BHSA	AX	N	D	Packing case
2	SPAKA8454BHZA	AN		D	Packing add R
3	SSAKH0003DHZZ	AE		D	Vinyl bag (640×560mm)
4	SPAKA8455BHZA	AN		D	Packing addL
5	SSAKH3015CCZZ	AA		D	Vinyl bag (200×300mm)
6	TiNSM2391BHZZ	BK	N	D	Instructiom book
7	SSAKA5004CCZZ	AA		D	Vinyl bag (100×300mm)
8	RCÖRF2336RCZZ	AC		C	HDD core [TQ,TS]
9	QCNW−7911RCZZ	BB		C	HDD cable [TQ,TS]
10	SSAKH4231CCZZ	AA		D	Vinyl sack (140×500)
11	TCADH6788BHZA	AC		D	Caution card (Black)
12	UBNDA6630BHZZ	AK		C	AC cord band
14	LKGiM1004BH01	AW		B	Clerk key(1) (2pcs/1set,with key ring)
	LKGiM1004BH02	AW		B	Clerk key(2) (2pcs/1set,with key ring)
	LKGiM1004BH03	AW		B	Clerk key(3) (2pcs/1set,with key ring)
	LKGiM1004BH04	AW		B	Clerk key(4) (2pcs/1set,with key ring)
	LKGiM1004BH05	AW		B	Clerk key(5) (2pcs/1set,with key ring)
	LKGiM1004BH06	AW		B	Clerk key(6) (2pcs/1set,with key ring)
15	PRNGT6641BHZZ	AE		C	Key ring
16	PSHEP2891BHZZ	AF	N	D	System sw label
17	XBBSD30P04000	AA		C	Screw (3×4) [TQ,TS]
18	LHLDZ2358RCZZ	AC		C	Holder (FRC-12CP) [TQ,TS]

3 Packing material & Accessories



4 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	RMPTQ4103QCJJ	AB		B	Block resistor (10KΩ×4 1/32W ±5%) [BR1,5,6,7,8,10,11,13,14]
	RMPTQ4103QCJJ	AB		B	Block resistor (10KΩ×4 1/32W ±5%) [BR16,17,18,19,22,23,25,29]
	RMPTQ4103QCJJ	AB		B	Block resistor (10KΩ×4 1/32W ±5%) [BR34,35,36,37,38,44,45,47]
	RMPTQ4103QCJJ	AB		B	Block resistor (10KΩ×4 1/32W ±5%) [BR48,49]
2	RMPTQ4472QCJJ	AC		B	Block resistor (4.7KΩ×4) [BR2]
3	RMPTQ2103QCJJ	AA		B	Block resistor (10KΩ×2) [BR3]
4	RMPTQ2472QCJJ	AA		B	Block resistor (4.7KΩ×2) [BR4]
5	RMPTQ4102QCJJ	AB		B	Block resistor (1KΩ×4) [BR9,12]
6	RMPTQ4473QCJJ	AB		B	Block resistor (47KΩ×4) [BR15]
7	RMPTQ4223QCJJ	AB		B	Block resistor (22KΩ×4 ±5%) [BR20,21,24]

4 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
8	RMPTQ4330QCJJ	AC		B	Block resistor (33Ω×4 1/16W ±5%)	[BR26,27,28,30,31,32,33]
9	RMPTQ4220QCJJ	AB		B	Block resistor (22Ω×4 1/32W ±5%)	[BR39,40,41,42,43,46]
10	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C1,2,3,11,13,35]
11	VCEAPS1EC476M	AF		C	Capacitor (25WV 47μF)	[C4,5,30,33]
12	VCEAPS1VC226M	AC		C	Capacitor (35WV 22μF)	[C8,10]
13	RC−CZ1063RC1A	AE		C	Capacitor (10WV 10μF)	[C12,21]
14	VCEAPS1CC106M	AC		C	Capacitor (16WV 10μF)	[C15,36]
15	VCTZZA0JD157M	AN		C	Capacitor (6.3WV 150μF)	[C16,29]
16	VCCCTV1HH180J	AA		C	Capacitor (50WV 18pF)	[C18]
17	VCCCTV1HH150J	AA		C	Capacitor (50WV 15PF)	[C19]
18	VCCCTV1HH270J	AC		C	Capacitor (50WV 27pF)	[C20]
19	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C22]
20	VCCCTV1HH100J	AA		C	Capacitor (50WV 10PF)	[C24,25,26]
21	VCCCTV1HH220J	AA		C	Capacitor (50WV 22PF)	[C27,28]
22	VHDSFPB72／／−1	AE		B	Diode (SFPB72)	[D1]
23	VHDSFPB54／／−1	AC		B	Diode (SFPB54)	[D2]
24	RCiLZ5017SCZZ	AB		C	Chip coil (BLM31)(RCILZ5017SCZ-)	[FB6,7,8,9,10,11,12,13,14]
	RCiLZ5017SCZZ	AB		C	Chip coil (BLM31)	[FB15,16,17,18,19,20,21,22]
	RCiLZ5017SCZZ	AB		C	Chip coil (BLM31)(RCILZ5017SCZ)	[FB23,24,25,26,27,28,29,30]
	RCiLZ5017SCZZ	AB		C	Chip coil (BLM31)(RCILZ5017SCZ-)	[FB31,32,33,34,35,36]
25	VHiMC145406F1	AL		B	IC (MC145406F)(VHIMC145406F-)	[IC2,3,4,7,8]
26	VHiMC14069UBD	AK		B	IC (MC14069UBD)	[IC5,34]
27	VHiSN74LS125R	AL		B	IC (SN74LS125DR D014 TAPPING)	[IC6,12,29,30]
28	VHiLZ9AM22／−1	BH		B	IC (PSC)(LZ9AM22)	[IC9]
29	VHiRN5VL45CA1	AF		B	IC (VOLT DETECTOR RX5VT SOP)(RX5VTXXC)	[IC10]
30	VHiSN75189DR／	AK		B	IC (SN75189DR)	[IC14]
31	VHiM5113A2QFP	BB		B	IC (M5113)	[IC15]
32	VHiSN74HC04DR	AG		B	IC (SN74HC04DR)	[IC16,20]
33	VHiM38802M270	BA		B	IC (M38802M270)	[IC17]
34	VHi51V8512T12	BG		B	IC (4M PSRAM)(TC51V8512AFT)	[IC18,19]
35	VHiSN74HC32DR	AG		B	IC (SN74HC32DR)	[IC21,33]
36	VHiSN74HC00DR	AG		B	IC (SN74HC00DR)	[IC22]
37	VHiSN74HC08DR	AL		B	IC (SN74HC08DR D014 TAPPING)	[IC23]
38	VHi74VHC04／−1	AE		B	IC (74VHC04)	[IC24]
39	VHi28F016SU10	BU		B	IC (FLASH ROM)(28F016SU10)	[IC25]
40	VHiLH535DVC−1	BA		B	Mask ROM (LH53V32500T)	[IC26]
41	VHiBQ3285ESS1	AW		B	IC (BQ3285ESS SOP)	[IC27]
42	VHi28F004SUT8	BA		B	IC (BIOS F-ROM)(LH28F004SUT)	[IC28]
43	VHiMAX797CSE／	AZ		B	IC (MAX797 SOP)	[IC31]
44	VHi82C700P／−1	BT		B	IC (82C700P)	[IC32]
45	VHi51W16165A6	BE		B	IC (16MB DRAM)(UPD4265165)	[IC35,36,37,38]
46	VHiMK1492−04R	AY		B	IC (MK1492-04)	[IC39]
47	VHiMAX1651／−1	AS		B	IC (MAX1651)	[IC41]
48	VHiRH5RE33A−1	AF		B	IC (VOLT REGULATOR RH5RE SOP)	[IC42]
49	RCiLC6665RCZZ	AH		C	Chip coil (CDRH127-3R5NC)3.5UH	[L2]
50	RCiLC6666RCZZ	AH		C	Coil (39μH SMD)	[L3]
51	VHHMiNSMDC020	AF		B	Thermistor (MiniSMD020-2)	[PF1,2]
52	VSDTA144EK／−1	AC		B	Digital transistor (DTA144EK)	[Q1,3]
53	VSDTC114YK／−1	AC		B	Transistor (DTC114YK)	[Q2,4]
54	VSSi9410DY／−1	AK		B	Transistor (SI 20V)(SI9410DY)	[Q5,6]
55	VSSi9430DY／−1	AL		B	Chip FET (SI9430DY)	[Q7]
56	VRS−TS2AD682J	AA		C	Resistor (1/10W 6.8KΩ ±5%)	[R1,2]
57	VRS−TS2AD471J	AA		C	Resistor (1/10W 470Ω ±5%)	[R3,4,5]
58	VRS−TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R7,14]
59	VRS−TS2AD106J	AA		C	Resistor (1/10W 10MΩ ±5%)	[R9,22]
60	VRS−TS2AD220J	AA		C	Resistor (1/10W 22Ω ±5%)	[R10]
61	VRS−TS2AD470J	AA		C	Resistor (1/10W 47Ω ±5%)	[R11,13]
62	VRS−TS2AD474J	AA		C	Resistor (1/10W 470KΩ ±5%)	[R12]
63	VRS−TS2AD330J	AA		C	Resistor (1/10W 33Ω ±5%)	[R15,16,17,18,19]
64	VRS−TS2AD105J	AA		C	Resistor (1/10W 1MΩ ±5%)	[R20,]
65	VRS−TS2AD000J	AA		C	Resistor (1/10W 0Ω ±5%)	[JR1]
	VRS−TS2AD000J	AA		C	Resistor (1/10W 0Ω ±5%)	[R21,6]
66	VRSTE2HFR025F	AE		C	Resistor (1/2W 0.025Ω ±1%)	[R8]
67	VRSTE2HFR033F	AE		C	Resistor (1/2W 0.033Ω ±1%)	[R23]
68	VRS−TS2AD154F	AA		C	Resistor (1/10W 150KΩ ±1%)	[R24]
69	VRS−TS2AD144F	AC		C	Resistor (1/10W 140KΩ ±1%)	[R25]
70	VRS−TS2HD130J	AD		C	Resistor (1/2W 13Ω ±5%)	[R26,27]
71	RCRMZ7004RCZZ	AE		B	Chip resonater (CSTCC 7.37MG)	[X1]
72	RCRMZ7003RCZZ	AF		B	Chip resonater (CSTCV24.00MX0H)	[X2]
73	RCRSZ6671RCZZ	AH		B	Crystal (32.768MHz,MA-306-SOJ)	[X3,4]
74	RCRSZ6670RCZZ	AK		B	Crystal (14.3181MHz,MA-406-SOJ)	[X5]
75	QCNCM2806RC8J	AR		C	Connector (80pin)(53489-0809)	[CN11]
76	QCNCW2612RCDD	AZ		C	SO DIMM socket (72P×2)	[CN5]
77	QSÖCZ2036HCZZ	AS		C	DIMM socket (SO DIMM 144pin)(54026-1440)	[CN13]
78	RCiLC2414RCZZ	AH		C	Coil (CD105 68μH)	[L4]
79	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C23]
80	VHi74HC138DR／	AK		B	IC (SN74HC138DR)	[IC11]
81	VHiBA10393F−1	AC		B	IC (BA10393F)	[IC13]
82	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C109,113,114,116,119,123,124,126]
	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C132,133,135,141,145,146,147,160]

4 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C161,173,177,180,185,187,189,191]
	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C125]
82	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C193,197,204,208,214,218,220,224]
	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C226,227,228,229,230,236,238,240]
	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF)	[C241,242,243,244]
83	VCCCTV1HH390J	AA		C	Capacitor (50WV 39pF)	[C252,253,254,255]
84	RC-CZ1063RC1A	AE		C	Capacitor (10WV 10μF)	[C198,199,206,207,216,217,219,225]
	RC-CZ1063RC1A	AE		C	Capacitor (10WV 10μF)	[C232,233,234,246]
	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C107,136,142,150,163,164,165,166]
85	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C167,170,171,172,182,184,192,196]
	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C200,203,205,209,210,211,212,213]
	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF)	[C215,221,222,223,231,235,237,239]
86	VCCCTV1HH100J	AA		C	Capacitor (50WV 10PF)	[C194,247,249,250,251]
	VCCCTV1HH221J	AA		C	Capacitor (50WV 220PF)	[C100,101,102,103,104,105,106,108]
87	VCCCTV1HH221J	AA		C	Capacitor (50WV 220PF)	[C110,111,112,115,118,120,121,122]
	VCCCTV1HH221J	AA		C	Capacitor (50WV 220PF)	[C130,168]
88	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF)	[C117,137,138,139,148,149,151,152]
	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF)	[C153,154,155,156,157,158,159]
89	VCCCTV1HH331J	AA		C	Capacitor (50WV 330pF)	[C127,128,129,131,144,181]
90	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF)	[C140,143,162,169,175,195]
91	VCKYTV1CF105Z	AB		C	Capacitor (16WV 1μF)	[C179,183,190,201,202,245]
92	VCKYTV1CB334K	AC		C	Capacitor (16WV 0.33μF)	[C186]
93	VCKYTV1HB103K	AB		C	Capacitor (50WV 0.010μF)	[C188]
94	VHD1SS353//-1	AB		B	Diode (1SS353)	[D100,101,102,103,104,105,106,107]
	VHD1SS353//-1	AB		B	Diode (1SS353)	[D108]
95	VHD1SS322//-1	AC		B	Diode (1SS322)	[D110]
	RCiLZ5017SCZZ	AB		C	Chip coil (BLM31)(RCILZ5017SCZ-)	[FB100,101,102,103,104,105,108]
96	RCiLZ5017SCZZ	AB		C	Chip coil (BLM31)(RCILZ5017SCZ-)	[FB111,112,113,119,120,106,107]
	RCiLZ5017SCZZ	AB		C	Chip coil (BLM31)(RCILZ5017SCZ-)	[FB109,110,115,116,117,118]
	RCŌRF1008ACZZ	AB		C	Chip bead (BLM21A05)	[FB114,121,122,123,124,125,126]
97	RCŌRF1008ACZZ	AB		C	Chip bead (BLM21A05)	[FB127,128,129,130,131,132,133]
	RCŌRF1008ACZZ	AB		C	Chip bead (BLM21A05)	[FB134,135,136,137,138,139,140]
	RCŌRF1008ACZZ	AB		C	Chip bead (BLM21A05)	[FB141,142,143,144,145,146,147]
98	VHViCPS1.0/-1	AF		B	IC protector (ICPS1.0)	[IF100]
99	VHDSFPB72//-1	AE		B	Diode (SFPB72)	[D109]
100	VSDTC114YK/-1	AC		B	Transistor (DTC114YK)	[Q101,102,103]
101	VSDTC124GK/-1	AC		B	Transistor (DTC124GK)	[Q100]
102	VS2SJ187-//-1	AF		B	Transistor (2SJ187)	[Q104]
103	VRS-TS2AD471J	AA		C	Resistor (1/10W 470Ω ±5%)	[R110,112,117,119,121]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R113,114,115,116,118,120,126,127]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R130,133,135,138,143,144,147,150]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R155,157,165,166,167,168,169,172]
104	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R173,174,177,178,180,184,185,186]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R187,188,190,191,192,193,194,195]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R197,198,199,202,205,206,210,211]
	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%)	[R212]
105	VRS-TS2AD220J	AA		C	Resistor (1/10W 22Ω ±5%)	[R107,162]
106	VRS-TS2AD330J	AA		C	Resistor (1/10W 33Ω ±5%)	[R156,179,215,216,217,218]
107	VRS-TS2AD000J	AA		C	Resistor (1/10W 0Ω ±5%)	[R201,207,JR100]
	VRS-TS2AD102J	AA		C	Resistor (1/10W 1.0KΩ ±5%)	[R100,122,123,124,125,128,129,132]
108	VRS-TS2AD102J	AA		C	Resistor (1/10W 1.0KΩ ±5%)	[R134,136,137,140,149,151,154,158]
	VRS-TS2AD102J	AA		C	Resistor (1/10W 1.0KΩ ±5%)	[R159,160,161,163,164,170,171,175]
	VRS-TS2AD102J	AA		C	Resistor (1/10W 1.0KΩ ±5%)	[R176]
109	VRS-TS2AD272J	AA		C	Resistor (1/10W 2.7KΩ ±5%)	[R101]
110	VRS-TS2AD473J	AA		C	Resistor (1/10W 47KΩ ±5%)	[R102]
111	VRS-TS2AD332J	AA		C	Resistor (1/10W 3.3KΩ ±5%)	[R104,148,111]
112	VRS-TS2AD122J	AA		C	Resistor (1/10W 1.2KΩ ±5%)	[R106]
113	VRS-TS2AD152J	AA		C	Resistor (1/10W 1.5KΩ ±5%)	[R152]
114	VRS-TS2AD270J	AA		C	Resistor (1/10W 27Ω ±5%)	[R181,182,183,189,196]
115	VRS-TS2AD223J	AA		C	Resistor (1/10W 22KΩ ±5%)	[R200,208]
116	VRS-TS2AD104J	AA		C	Resistor (1/10W 100KΩ ±5%)	[R105]
117	VRS-TS2AD822J	AA		C	Resistor (1/10W 8.2KΩ ±5%)	[R209]
118	VRS-TS2AD751J	AA		C	Resistor (1/10W 750Ω ±5%)	[R213,214]
119	VRS-TS2AD105J	AA		C	Resistor (1/10W 1MΩ ±5%)	[R141]
120	VCCCTV1HH471J	AA		C	Capacitor (50WV 470pF)	[C174,176,178]
121	VRS-TS2AD222J	AA		C	Resistor (1/10W 2.2KΩ ±5%)	[R109]
122	VRS-TS2AD472J	AA		C	Resistor (1/10W 4.7KΩ ±5%)	[R108]
123	QCNCM7176BH0G	AD		C	Connector (53014-0710)	[CN1]
124	QCNCW2811BH1F	AM		C	Connector (52030-1610)	[CN2]
125	QCNCM7142BH1B	AD		C	WMF Connector (GIL-G-12P-S3T2-E)	[CN3,15]
126	QCNCM7221BH1J	AL		C	Connector (MLX 53047-1010)	[CN4]
127	VHiA80502-133	CS		B	IC (CPU)(A80502-133)	[IC40]
128	QCNCM7128BH1E	AH		C	Connector (MLX 53047-1510)	[CN6]
129	QCNCM7222BH0C	AC		C	Connector (MLX 53014-0310)	[CN7,9]
130	QCNCW7040RCAJ	AT		C	Connector (100pin)(8801-100-170S KEL)	[CN8]
131	VHi4AC16///-1	AK		B	IC (4AC16)	[IC1]
132	QCNCW7081BHZZ	AB		C	Connector (2P)(5267-02A)(Blue)	[CN16]
133	RALMB6640RCZZ	AF		B	Buzzer (SM×06)	[BZ1]
134	RC-EZ106ARC1A	AD		C	Capacitor (10WV 10μF)	[C6,7,17]
135	RC-EZ2271RC1A	AM		C	Capacitor (6.3WV 220μF)	[C9]

4 Main PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
136	RC-EZ1072RC1A	AN		C	Capacitor (10WV 100μF) [C14,34]
137	RC-EZ1572RC0J	AN		C	Capacitor (6.3WV 150μF SL) [C31,32]
138	RCŌRF6691BHZZ	AD		C	Core (BFS3550R2F) [FB1,38,39]
139	RCiLF0050FCZZ	AG		C	Ferrite bead (C66663) [FB2,3,4,5]
140	RCŌRF6706BHZZ	AD		C	Bead core (BFS3580A0) [FB37]
141	QSW-S0744AFZZ	AG		B	Reset switch (SSS312) [S1,2]
142	RCiLC6662RCZZ	AK		C	Coil (10μH/3A) [L1]
⚠ 143	QFS-G4302QCZZ	AG		A	Fuse (3.15A/125V) [F1]
144	RC-EZ476ARC1A	AF		C	Capacitor (47μF/10V) [C37]
145	VCEAGU0JW227M	AB		C	Capacitor (6.3WV 220μF SS) [C38]
146	QCNW-3034BHZZ	AK		C	Earth wire [J1]
147	QCNCW2811BH1B	AK		C	Connector (52030-1210) [CN10]
148	QCNCM7176BH0H	AD		C	Connector (KEY)(5394-0810) [CN14]
149	QCNCM7057BH08	AG		C	Connector (MLX 5045-0810) [CN100]
150	QCNCW2805RC0H	AU		C	Connector (TM11R-3C-88) [CN101,102,107]
151	QCNCM2788BH0i	BL		C	Connector (D-SUB 9pin)(Straight type) [CN103,104]
152	QCNCM7057BHZZ	AB		C	Connector (5045-3)(3pin) [CN105,106]
153	QCNCM6467RC4D	AN		C	Connector (A3E-44A-2DSA) [CN108]
154	QCNCM7176BH1J	AD		C	Connector (53014-1010)(10pin) [CN109]
155	QCNCW7283BH2F	AS		C	Connector (5597-26CPB) [CN110]
156	RVR-B5310QCZZ	AG		B	Volume (20K) [VR1,2]
	(Unit)				
901	CPWBX2826BH03	DT	N	E	Main PWB unit

5 VGA PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	RMPTQ4330QCJJ	AC		B	Block resistor (33Ω×4 1/16W ±5%) [BR301]
	RMPTQ4330QCJJ	AC		B	Block resistor (33Ω×4 1/16W ±5%) [BR302,303,304]
2	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF) [C300]
3	RC-CZ1063RC1A	AE		C	Capacitor (10WV 10μF) [C302,303]
4	VCKYTV1CF105Z	AB		C	Capacitor (16WV 1μF) [C301]
5	RCiLZ5017SCZZ	AB		C	Chip coil (BLM31)(RCILZ5017SCZ-) [FB301,309]
	RCiLZ5017SCZZ	AB		C	Chip coil (BLM31)(RCILZ5017SCZ-) [FB310]
6	VHViCPS1.0/-1	AF		B	IC protector (ICPS1.0) [IF300]
7	QCNCW2807RC8J	AS		C	Connector (80pin)(52775-0809) [CN300]
8	RCŌRF2327RCZZ	AE		C	Chip core (ACA3216M4S-120) [FB300,302,303,307,308]
9	VHi416V254TL6	AX		B	IC (4MB DRAM)(416V254DT-L6) [IC300,301]
10	VHi74HCT244AF	AK		B	IC (74HCT244) [IC302,306,307]
11	VHi74HCT08ANS	AE		B	IC (74HCT08) [IC303]
12	VHi74HCT00ANS	AH		B	IC (74HCT00) [IC304]
13	VHiMN89305/-1	BG		B	IC (MN89305) [IC305]
14	RCRSZ2402RCZZ	AL	N	B	X-TAL (18.00MHz) [X300]
15	VRS-TS2AD334J	AA		C	Resistor (1/10W 330KΩ ±5%) [R300]
16	VS2SJ187-//-1	AF		B	Transistor (2SJ187) [Q300]
17	RCŌRF1008ACZZ	AB		C	Chip bead (BLM21A05) [FB304,305,306]
18	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF) [C400,402,407,408]
	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF) [C409,410]
19	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF) [C401,403,406]
20	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF) [C411]
	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF) [C412,413,414,415,416,417,418,419]
	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF) [C420,421,422,423,424,425,426,427]
	VCCCTV1HH470J	AA		C	Capacitor (50WV 47PF) [C428,429,430]
21	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R401,402,409]
22	VRS-TS2AD330J	AA		C	Resistor (1/10W 33Ω ±5%) [R405]
23	VRS-TS2AD102J	AA		C	Resistor (1/10W 1.0KΩ ±5%) [R403]
24	VRS-TS2AD333J	AA		C	Resistor (1/10W 33KΩ ±5%) [R400]
25	VRS-TS2AD183J	AA		C	Resister (1/10W 18KΩ ±5%) [R404]
26	VCCCTV1HH240J	AA		C	Capacitor (50WV 24pF) [C405]
27	VCCCTV1HH270J	AC		C	Capacitor (50WV 27pF) [C404]
28	QCNCM7207BH4J	AQ		C	Connector (40P)(6229ZiF DIP) [CN400]
	(Unit)				
901	CPWBX2827BH02	CF	N	E	VGA PWB unit

6 Touch panel PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCM7207BH4J	AQ		C	Connector (40P)(6229ZiF DIP) [CN5]
2	QCNCM7226BH0E	AD		C	Connector (MLX53015-0510) [CN4]
3	QCNCM7230BH1E	AL		C	Connector (00-6200-157-012-800) [CN1]
4	RC-KZ1054CCZZ	AB		C	Capacitor (10WV 0.1μF) [C24,25]
5	QCNW-2994BHZZ	AE		C	GND wire
6	RC-EZ106ARC1A	AD		C	Capacitor (10WV 10μF) [C26]
7	RC-EZ1572RC0J	AN		C	Capacitor (6.3WV 150μF SL) [C12]
8	QCNCW2812BH3J	AP		C	Connector (MLX 52437-3091) [CN3]
9	RCiLZ5017SCZZ	AB		C	Chip coil (BLM31) [FB1,3,5]
10	RCRMZ7002RCZZ	AE		B	Crystal (8 MHz) [X1]
11	VCCCTV1HH331J	AA		C	Capacitor (50WV 330pF) [C15,16]
12	VCCCTV1HH681J	AA		C	Capacitor (50WV 680PF) [C1]
13	VCEAPS1CC336M	AF		C	Capacitor (16WV 33μF) [C10,11]
14	VCKYTV1HB182K	AA		C	Capacitor (50WV 1800PF) [C3,4,5,6]
15	VCKYTV1HB472K	AA		C	Capacitor (50WV 4700pF) [C2]
16	VCKYTV1HF104Z	AA		C	Capacitor (50WV 0.10μF) [C7,8,9]
17	VHD1SS353//-1	AB		B	Diode (1SS353) [D1,2,3,4,5,6,7,8,9,10,11,12,13]
	VHD1SS353//-1	AB		B	Diode (1SS353) [D14]
18	VHiM89635N010	BA		B	IC (MB89635R) [IC2]
19	VHiS29390AFJA	AL		B	IC (E2PROM)(S-29390AF) [IC1]
20	VRS-TQ2BB000J	AA		C	Resistor (1/8W 0Ω ±5%) [FB2,4]
21	VRS-TS2AD102J	AA		C	Resistor (1/10W 1.0KΩ ±5%) [R2]
22	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R4,5,6,7,8,9,10]
23	VRS-TS2AD203J	AA		C	Resistor (1/10W 20KΩ ±5%) [R3]
24	VRS-TS2AD822J	AA		C	Resistor (1/10W 8.2KΩ ±5%) [R1]
25	VSDTA124EK//-1	AD		B	Transistor (DTA124EKA) [Q1,3,5]
26	VSDTC124TK//-1	AD		B	Transistor (DTC124TKA) [Q2,4]
27	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF) [C14]
28	VCCCTV1HH180J	AA		C	Capacitor (50WV 18PF) [C27,28]
29	RCiLZ1051LCZZ	AD		C	Coil (LQH 3C) [L1]
	(Unit)				
901	CPWBN2836BH01	BR		E	Touch panel PWB unit

7 Inverter PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCM2656RC0C	AE		C	Connector (BHR-03VS-1) [CN501A]
2	RC-CZ2201RC0F	AE		C	Capacitor (22pF/3.15KV) [C504A]
3	RCiLC6667BHZZ	AN		C	Coil (A814AY-101K)(100μH SMD) [L501A]
⚠ 4	RTRNH9521BHZZ	BB		B	Transformer (841TN-1157) [T501A]
5	VHiLT1184CS-1	BE		B	IC (LT1184) [IC501A]
6	VCEAPS1CC225M	AF		C	Capacitor (2.2μF/16V) [C501A]
7	VCEAPS1CC226M	AC		C	Capacitor (16WV 22μF) [C502A]
8	VRS-TS2AD133F	AA		C	Resistor (1/10W 13KΩ ±1%) [R501A]
9	VRS-TS2AD472J	AA		C	Resistor (1/10W 4.7KΩ ±5%) [R502A]
10	RC-FZ8231RC2A	AG		C	Capacitor (0.082μF/100V) [C601A]
11	VCKYTV1CF105Z	AB		C	Capacitor (16WV 1μF) [C602A]
12	VCKYTV1HB102K	AA		C	Capacitor (50WV 1000PF) [C103]
13	VHDSFPB54//-1	AC		B	Diode (SFPB54) [D601A,602A]
14	VHViCPS0.5/-1	AF		B	IC-protector (ICPS0.5) [F601A]
15	VRS-TS2AD104J	AA		C	Resistor (1/10W 100KΩ ±5%) [R601A]
16	VRS-TS2AD222J	AA		C	Resistor (1/10W 2.2KΩ ±5%) [R603A,604A]
17	VRS-TS2AD224J	AA		C	Resistor (1/10W 220KΩ ±5%) [R602A]
18	VS2SD2391//-1	AD		B	Transistor (2SD2391Q) [Q601A,602A]
19	QCNCM7226BH0E	AD		C	Connector (MLX53015-0510) [CN502]
	(Unit)				
901	CPWBN2794BH01	BQ		E	Inverter PWB unit

8 Riser PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCM7126BH2B	AN		C	AT Connector (HRS PCC-22C 98P) [CN1,2]
2	QCNCM7037RCAJ	AT		C	ISA Connector (100pin)(8811-100-170L) [CN3]
3	VCEAGA1HW226M	AB		C	Capacitor (50WV 22μF) [C1,2,3]
4	QSW-S0744AFZZ	AG		B	Reset switch (SSS312) [S12]
5	VHDSB140///-1	AF		B	Diode (SB140)
6	VRS-TS2AD272J	AA		C	Resistor (1/10W 2.7KΩ ±5%) [R104,105,106,108]
7	VRS-TS2AD103J	AA		C	Resistor (1/10W 10KΩ ±5%) [R113,114]
8	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF) [C102,103,104,105,106,107,108,109]
	VCCCTV1HH101J	AA		C	Capacitor (50WV 100PF) [C110,111,112,113,114,115,116,117]
	(Unit)				
901	CPWBX2835BH01	BQ		E	Riser PWB unit

9 SW PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCW1275AC0F	AF		C	Connector (TCS7567-01-401) [CN202]
2	QCNCW2811BH1F	AM		C	Connector (52030-1610) [CN201]
3	QSW-Z6909BHZZ	AF		B	Reset switch (JIP1236HA) [S201]
4	QSW-Z7011XCZZ	AL		B	Dip switch (DPS-8-E) [S202]
	(Unit)				
901	CPWBN2829BH01	BA		E	Switch PWB unit

10 LCD PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCW1230AC3A	AK		C	Connector (31pin)(CL540 0063-0-31) [CN1]
2	QCNCW2812BH3J	AP		C	Connector (MLX 52437-3091) [CN2]
	(Unit)				
901	CPWBN2789BH02	AY		E	LCD PWB unit

11 Service route options & Service tools

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNW-7858BHZZ	BL		S	Connector cable for Dongle (LPT-1) [Relay line from terminal to Dongle]
2	DKiT-8671RCZZ			S	HDD mounting kit (Bracked assembly for mounting) [KB]
11	GCÖVH7163BHSA	AR	N	D	FDD cover
12	LANGK2840BHZZ	AK		C	FDD angle
13	LPLTM2356BHZZ	AL		C	FDD sh plate
14	GCÖVH7171BHSA	AQ	N	D	FDD F cover
51	GCÖVH7138BHZZ	AL		D	HDD cover A [KB]
52	GCÖVH7139BHZZ	AN		D	HDD cover B [KB]
53	LANGK7620BHZZ	AE		C	HDD plate [KB]
54	PCUSG7080RCZZ	AH		C	HDD cushion [KB]
55	LX-BZ6794BHZZ	AE		C	Screw (M3×14) [KB]
101	DKiT-8656BHZZ			S	Service tool kit [ISA checker,ISA relay board ,RAM relay board]
102	UKÖG-6717RCZZ	BR		S	Printer connector signal loop back connector [for ER-A8RS CENTRONICS connector]
103	UKÖG-6718RCZZ	BE		S	MCR test card [for UP-E12MR2]
104	UKÖG-6705RCZZ	BC		S	RS232 loop back connector [for RS232 connector]
105	CKÖG-6727BHZZ	CS		S	BIOS loading board [for overwriting BIOS]
106	UKÖG-6729BHZZ	AZ		S	RS232 moduler jack loop back connector [for RJ45 connector]
111	LKGiM1004BH07	BH		S	Clerk key(7) (2pcs/1set,with key ring)
112	LKGiM1004BH08	BH		S	Clerk key(8) (2pcs/1set,with key ring)
113	LKGiM1004BH09	BH		S	Clerk key(9) (2pcs/1set,with key ring)
114	LKGiM1004BH10	BH		S	Clerk key(10) (2pcs/1set,with key ring)
115	LKGiM1004BH11	BH		S	Clerk key(11) (2pcs/1set,with key ring)
116	LKGiM1004BH12	BH		S	Clerk key(12) (2pcs/1set,with key ring)
117	LKGiM1004BH13	BH		S	Clerk key(13) (2pcs/1set,with key ring)
118	LKGiM1004BH14	BH		S	Clerk key(14) (2pcs/1set,with key ring)
119	LKGiM1004BH15	BH		S	Clerk key(15) (2pcs/1set,with key ring)
120	LKGiM1004BH16	BH		S	Clerk key(16) (2pcs/1set,with key ring)
121	LKGiM1004BH17	BH		S	Clerk key(17) (2pcs/1set,with key ring)
122	LKGiM1004BH18	BH		S	Clerk key(18) (2pcs/1set,with key ring)
123	LKGiM1004BH19	BH		S	Clerk key(19) (2pcs/1set,with key ring)
124	LKGiM1004BH20	BH		S	Clerk key(20) (2pcs/1set,with key ring)
125	LKGiM1004BH21	BH		S	Clerk key(21) (2pcs/1set,with key ring)
126	LKGiM1004BH22	BH		S	Clerk key(22) (2pcs/1set,with key ring)
127	LKGiM1004BH23	BH		S	Clerk key(23) (2pcs/1set,with key ring)
128	LKGiM1004BH24	BH		S	Clerk key(24) (2pcs/1set,with key ring)
129	LKGiM1004BH25	BH		S	Clerk key(25) (2pcs/1set,with key ring)
130	LKGiM1004BH26	BH		S	Clerk key(26) (2pcs/1set,with key ring)
131	LKGiM1004BH27	BH		S	Clerk key(27) (2pcs/1set,with key ring)
132	LKGiM1004BH28	BH		S	Clerk key(28) (2pcs/1set,with key ring)
133	LKGiM1004BH29	BH		S	Clerk key(29) (2pcs/1set,with key ring)
134	LKGiM1004BH30	BH		S	Clerk key(30) (2pcs/1set,with key ring)
135	LKGiM1004BH31	BH		S	Clerk key(31) (2pcs/1set,with key ring)
136	LKGiM1004BH32	BH		S	Clerk key(32) (2pcs/1set,with key ring)
137	LKGiM1004BH33	BH		S	Clerk key(33) (2pcs/1set,with key ring)
138	LKGiM1004BH34	BH		S	Clerk key(34) (2pcs/1set,with key ring)
139	LKGiM1004BH35	BH		S	Clerk key(35) (2pcs/1set,with key ring)
140	LKGiM1004BH36	BH		S	Clerk key(36) (2pcs/1set,with key ring)
141	LKGiM1004BH37	BH		S	Clerk key(37) (2pcs/1set,with key ring)
142	LKGiM1004BH38	BH		S	Clerk key(38) (2pcs/1set,with key ring)
143	LKGiM1004BH39	BH		S	Clerk key(39) (2pcs/1set,with key ring)
144	LKGiM1004BH40	BH		S	Clerk key(40) (2pcs/1set,with key ring)
145	LKGiM1004BH41	BH		S	Clerk key(41) (2pcs/1set,with key ring)
146	LKGiM1004BH42	BH		S	Clerk key(42) (2pcs/1set,with key ring)
147	LKGiM1004BH43	BH		S	Clerk key(43) (2pcs/1set,with key ring)
148	LKGiM1004BH44	BH		S	Clerk key(44) (2pcs/1set,with key ring)
149	LKGiM1004BH45	BH		S	Clerk key(45) (2pcs/1set,with key ring)
150	LKGiM1004BH46	BH		S	Clerk key(46) (2pcs/1set,with key ring)
151	LKGiM1004BH47	BH		S	Clerk key(47) (2pcs/1set,with key ring)

11 Service route options & Service tools

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
152	LKGiM1004BH48	BH		S	Clerk key(48) (2pcs/1set,with key ring)
153	LKGiM1004BH49	BH		S	Clerk key(49) (2pcs/1set,with key ring)
154	LKGiM1004BH50	BH		S	Clerk key(50) (2pcs/1set,with key ring)
155	LKGiM1004BH51	BH		S	Clerk key(51) (2pcs/1set,with key ring)
156	LKGiM1004BH52	BH		S	Clerk key(52) (2pcs/1set,with key ring)
157	LKGiM1004BH53	BH		S	Clerk key(53) (2pcs/1set,with key ring)
158	LKGiM1004BH54	BH		S	Clerk key(54) (2pcs/1set,with key ring)
159	LKGiM1004BH55	BH		S	Clerk key(55) (2pcs/1set,with key ring)
160	LKGiM1004BH56	BH		S	Clerk key(56) (2pcs/1set,with key ring)
161	LKGiM1004BH57	BH		S	Clerk key(57) (2pcs/1set,with key ring)
162	LKGiM1004BH58	BH		S	Clerk key(58) (2pcs/1set,with key ring)
163	LKGiM1004BH59	BH		S	Clerk key(59) (2pcs/1set,with key ring)
164	LKGiM1004BH60	BH		S	Clerk key(60) (2pcs/1set,with key ring)
165	LKGiM1004BH61	BH		S	Clerk key(61) (2pcs/1set,with key ring)
166	LKGiM1004BH62	BH		S	Clerk key(62) (2pcs/1set,with key ring)
167	LKGiM1004BH63	BH		S	Clerk key(63) (2pcs/1set,with key ring)
168	LKGiM1004BH64	BH		S	Clerk key(64) (2pcs/1set,with key ring)
169	LKGiM1004BH65	BH		S	Clerk key(65) (2pcs/1set,with key ring)
170	LKGiM1004BH66	BH		S	Clerk key(66) (2pcs/1set,with key ring)
171	LKGiM1004BH67	BH		S	Clerk key(67) (2pcs/1set,with key ring)
172	LKGiM1004BH68	BH		S	Clerk key(68) (2pcs/1set,with key ring)
173	LKGiM1004BH69	BH		S	Clerk key(69) (2pcs/1set,with key ring)
174	LKGiM1004BH70	BH		S	Clerk key(70) (2pcs/1set,with key ring)
175	LKGiM1004BH71	BH		S	Clerk key(71) (2pcs/1set,with key ring)
176	LKGiM1004BH72	BH		S	Clerk key(72) (2pcs/1set,with key ring)
177	LKGiM1004BH73	BH		S	Clerk key(73) (2pcs/1set,with key ring)
178	LKGiM1004BH74	BH		S	Clerk key(74) (2pcs/1set,with key ring)
179	LKGiM1004BH75	BH		S	Clerk key(75) (2pcs/1set,with key ring)
180	LKGiM1004BH76	BH		S	Clerk key(76) (2pcs/1set,with key ring)
181	LKGiM1004BH77	BH		S	Clerk key(77) (2pcs/1set,with key ring)
182	LKGiM1004BH78	BH		S	Clerk key(78) (2pcs/1set,with key ring)
183	LKGiM1004BH79	BH		S	Clerk key(79) (2pcs/1set,with key ring)
184	LKGiM1004BH80	BH		S	Clerk key(80) (2pcs/1set,with key ring)
185	LKGiM1004BH81	BH		S	Clerk key(81) (2pcs/1set,with key ring)
186	LKGiM1004BH82	BH		S	Clerk key(82) (2pcs/1set,with key ring)
187	LKGiM1004BH83	BH		S	Clerk key(83) (2pcs/1set,with key ring)
188	LKGiM1004BH84	BH		S	Clerk key(84) (2pcs/1set,with key ring)
189	LKGiM1004BH85	BH		S	Clerk key(85) (2pcs/1set,with key ring)
190	LKGiM1004BH86	BH		S	Clerk key(86) (2pcs/1set,with key ring)
191	LKGiM1004BH87	BH		S	Clerk key(87) (2pcs/1set,with key ring)
192	LKGiM1004BH88	BH		S	Clerk key(88) (2pcs/1set,with key ring)
193	LKGiM1004BH89	BH		S	Clerk key(89) (2pcs/1set,with key ring)
194	LKGiM1004BH90	BH		S	Clerk key(90) (2pcs/1set,with key ring)
195	LKGiM1004BH91	BH		S	Clerk key(91) (2pcs/1set,with key ring)
196	LKGiM1004BH92	BH		S	Clerk key(92) (2pcs/1set,with key ring)
197	LKGiM1004BH93	BH		S	Clerk key(93) (2pcs/1set,with key ring)
198	LKGiM1004BH94	BH		S	Clerk key(94) (2pcs/1set,with key ring)
199	LKGiM1004BH95	BH		S	Clerk key(95) (2pcs/1set,with key ring)
200	LKGiM1004BH96	BH		S	Clerk key(96) (2pcs/1set,with key ring)
201	LKGiM1004BH97	BH		S	Clerk key(97) (2pcs/1set,with key ring)
202	LKGiM1004BH98	BH		S	Clerk key(98) (2pcs/1set,with key ring)
203	LKGiM1004BH99	BH		S	Clerk key(99) (2pcs/1set,with key ring)
204	LKGiM1004BH00	BH		S	Clerk key(100) (2pcs/1set,with key ring)
205	LKGiM1004BHA1	BH		S	Clerk key(101) (2pcs/1set,with key ring)
206	LKGiM1004BHA2	BH		S	Clerk key(102) (2pcs/1set,with key ring)
207	LKGiM1004BHA3	BH		S	Clerk key(103) (2pcs/1set,with key ring)
208	LKGiM1004BHA4	BH		S	Clerk key(104) (2pcs/1set,with key ring)
209	LKGiM1004BHA5	BH		S	Clerk key(105) (2pcs/1set,with key ring)
210	LKGiM1004BHA6	BH		S	Clerk key(106) (2pcs/1set,with key ring)
211	LKGiM1004BHA7	BH		S	Clerk key(107) (2pcs/1set,with key ring)
212	LKGiM1004BHA8	BH		S	Clerk key(108) (2pcs/1set,with key ring)
213	LKGiM1004BHA9	BH		S	Clerk key(109) (2pcs/1set,with key ring)
214	LKGiM1004BHA0	BH		S	Clerk key(110) (2pcs/1set,with key ring)
215	LKGiM1004BHB1	BH		S	Clerk key(111) (2pcs/1set,with key ring)
216	LKGiM1004BHB2	BH		S	Clerk key(112) (2pcs/1set,with key ring)
217	LKGiM1004BHB3	BH		S	Clerk key(113) (2pcs/1set,with key ring)
218	LKGiM1004BHB4	BH		S	Clerk key(114) (2pcs/1set,with key ring)
219	LKGiM1004BHB5	BH		S	Clerk key(115) (2pcs/1set,with key ring)
220	LKGiM1004BHB6	BH		S	Clerk key(116) (2pcs/1set,with key ring)
221	LKGiM1004BHB7	BH		S	Clerk key(117) (2pcs/1set,with key ring)
222	LKGiM1004BHB8	BH		S	Clerk key(118) (2pcs/1set,with key ring)
223	LKGiM1004BHB9	BH		S	Clerk key(119) (2pcs/1set,with key ring)
224	LKGiM1004BHB0	BH		S	Clerk key(120) (2pcs/1set,with key ring)
225	LKGiM1004BHC1	BH		S	Clerk key(121) (2pcs/1set,with key ring)
226	LKGiM1004BHC2	BH		S	Clerk key(122) (2pcs/1set,with key ring)
227	LKGiM1004BHC3	BH		S	Clerk key(123) (2pcs/1set,with key ring)
228	LKGiM1004BHC4	BH		S	Clerk key(124) (2pcs/1set,with key ring)
229	LKGiM1004BHC5	BH		S	Clerk key(125) (2pcs/1set,with key ring)
230	LKGiM1004BHC6	BH		S	Clerk key(126) (2pcs/1set,with key ring)

■ Index

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
【C】					
CKŌG-6727BHZZ	11-105	CS		S	
CPWBN2789BH02	1- 21	AY		E	
〃	10-901	AY		E	
CPWBN2794BH01	1- 25	BQ		E	
〃	7-901	BQ		E	
CPWBN2829BH01	2- 35	BA		E	
〃	9-901	BA		E	
CPWBN2836BH01	1- 23	BR		E	
〃	6-901	BR		E	
CPWBX2826BH03	2- 30	DT	N	E	
〃	4-901	DT	N	E	
CPWBX2827BH02	2- 29	CF	N	E	
〃	5-901	CF	N	E	
CPWBX2835BH01	2- 12	BQ		E	
〃	8-901	BQ		E	
【D】					
DKiT-8656BHZZ	11-101			S	
DKiT-8671RCZZ	11- 2			S	
【G】					
GCABA7871BHSA	2- 38	BV		D	
GCABB7870BHSA	1- 41	BV		D	
GCABE7872BHSA	1- 34	BL		D	
GCABF7873BHSA	1- 7	BP		D	
GCŌVA7158BHSA	1- 48	BG		D	
GCŌVA7159BHSA	1- 35	BD		D	
GCŌVA7166BHZZ	1- 37	AP		D	
GCŌVH2472BHZZ	2- 42	BA		D	
GCŌVH7138BHZZ	2- 70	AL		D	
〃	11- 51	AL		D	
GCŌVH7139BHZZ	2- 72	AN		D	
〃	11- 52	AN		D	
GCŌVH7160BHZZ	2- 46	AN		D	
GCŌVH7161BHZZ	2- 56	AN		D	
GCŌVH7163BHSA	11- 11	AR	N	D	
GCŌVH7167BHZZ	1- 24	AH		D	
GCŌVH7168BHZZ	2- 21	AZ		D	
GCŌVH7171BHSA	11- 14	AQ	N	D	
GFTAT6927BHZB	1- 42	BD		D	
GFTAT6928BHZZ	1- 47	AV		D	
GFTAU2426BHZZ	2- 43	AR		D	
GLEGG6659BHZZ	2- 53	AE		D	
GSTN-2005BHZZ	1- 1	AT		C	
【H】					
HPNLC6839RCZZ	1- 31	BT		D	
【J】					
JKNBZ2411BHZZ	1- 2	AH		C	
JKNBZ6923BHZZ	1- 40	AP		C	
【L】					
LANGK2839BHZZ	2- 3	AR		C	
LANGK2840BHZZ	11- 12	AK		C	
LANGK7620BHZZ	2- 68	AE		C	
〃	11- 53	AE		C	
LANGK7649BHZZ	1- 17	AV		C	
LANGK7650BHZZ	1- 46	AH		C	
LANGK7651BHZZ	1- 36	AL		C	
LANGK7657BHZZ	2- 62	AK		C	
LANGT2808BHZZ	2- 9	AK		C	
LANGT2847BHZZ	1- 53	AP		C	
LANGT7637BHZZ	2- 11	AT		C	
LANGT7638BHZZ	2- 8	AM		C	
LBNDJ0007UCZZ	2- 76	AB		C	
LBNDJ2003SCZZ	2- 22	AA		C	
LCHSM6709BHZA	2- 36	AY		C	
LHLDK6847BHZZ	2- 54	AN		C	
LHLDW0006SCZZ	2- 39	AB		C	
LHLDW6821BHZZ	1- 55	AD		C	
LHLDZ2358RCZZ	3- 18	AC		C	
LKGiM1004BH00	11-204	BH		S	
LKGiM1004BH01	3- 14	AW		B	
LKGiM1004BH02	3- 14	AW		B	
LKGiM1004BH03	3- 14	AW		B	
LKGiM1004BH04	3- 14	AW		B	
LKGiM1004BH05	3- 14	AW		B	
LKGiM1004BH06	3- 14	AW		B	
LKGiM1004BH07	11-111	BH		S	
LKGiM1004BH08	11-112	BH		S	
LKGiM1004BH09	11-113	BH		S	
LKGiM1004BH10	11-114	BH		S	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
LKGiM1004BH11	11-115	BH		S	
LKGiM1004BH12	11-116	BH		S	
LKGiM1004BH13	11-117	BH		S	
LKGiM1004BH14	11-118	BH		S	
LKGiM1004BH15	11-119	BH		S	
LKGiM1004BH16	11-120	BH		S	
LKGiM1004BH17	11-121	BH		S	
LKGiM1004BH18	11-122	BH		S	
LKGiM1004BH19	11-123	BH		S	
LKGiM1004BH20	11-124	BH		S	
LKGiM1004BH21	11-125	BH		S	
LKGiM1004BH22	11-126	BH		S	
LKGiM1004BH23	11-127	BH		S	
LKGiM1004BH24	11-128	BH		S	
LKGiM1004BH25	11-129	BH		S	
LKGiM1004BH26	11-130	BH		S	
LKGiM1004BH27	11-131	BH		S	
LKGiM1004BH28	11-132	BH		S	
LKGiM1004BH29	11-133	BH		S	
LKGiM1004BH30	11-134	BH		S	
LKGiM1004BH31	11-135	BH		S	
LKGiM1004BH32	11-136	BH		S	
LKGiM1004BH33	11-137	BH		S	
LKGiM1004BH34	11-138	BH		S	
LKGiM1004BH35	11-139	BH		S	
LKGiM1004BH36	11-140	BH		S	
LKGiM1004BH37	11-141	BH		S	
LKGiM1004BH38	11-142	BH		S	
LKGiM1004BH39	11-143	BH		S	
LKGiM1004BH40	11-144	BH		S	
LKGiM1004BH41	11-145	BH		S	
LKGiM1004BH42	11-146	BH		S	
LKGiM1004BH43	11-147	BH		S	
LKGiM1004BH44	11-148	BH		S	
LKGiM1004BH45	11-149	BH		S	
LKGiM1004BH46	11-150	BH		S	
LKGiM1004BH47	11-151	BH		S	
LKGiM1004BH48	11-152	BH		S	
LKGiM1004BH49	11-153	BH		S	
LKGiM1004BH50	11-154	BH		S	
LKGiM1004BH51	11-155	BH		S	
LKGiM1004BH52	11-156	BH		S	
LKGiM1004BH53	11-157	BH		S	
LKGiM1004BH54	11-158	BH		S	
LKGiM1004BH55	11-159	BH		S	
LKGiM1004BH56	11-160	BH		S	
LKGiM1004BH57	11-161	BH		S	
LKGiM1004BH58	11-162	BH		S	
LKGiM1004BH59	11-163	BH		S	
LKGiM1004BH60	11-164	BH		S	
LKGiM1004BH61	11-165	BH		S	
LKGiM1004BH62	11-166	BH		S	
LKGiM1004BH63	11-167	BH		S	
LKGiM1004BH64	11-168	BH		S	
LKGiM1004BH65	11-169	BH		S	
LKGiM1004BH66	11-170	BH		S	
LKGiM1004BH67	11-171	BH		S	
LKGiM1004BH68	11-172	BH		S	
LKGiM1004BH69	11-173	BH		S	
LKGiM1004BH70	11-174	BH		S	
LKGiM1004BH71	11-175	BH		S	
LKGiM1004BH72	11-176	BH		S	
LKGiM1004BH73	11-177	BH		S	
LKGiM1004BH74	11-178	BH		S	
LKGiM1004BH75	11-179	BH		S	
LKGiM1004BH76	11-180	BH		S	
LKGiM1004BH77	11-181	BH		S	
LKGiM1004BH78	11-182	BH		S	
LKGiM1004BH79	11-183	BH		S	
LKGiM1004BH80	11-184	BH		S	
LKGiM1004BH81	11-185	BH		S	
LKGiM1004BH82	11-186	BH		S	
LKGiM1004BH83	11-187	BH		S	
LKGiM1004BH84	11-188	BH		S	
LKGiM1004BH85	11-189	BH		S	
LKGiM1004BH86	11-190	BH		S	
LKGiM1004BH87	11-191	BH		S	
LKGiM1004BH88	11-192	BH		S	
LKGiM1004BH89	11-193	BH		S	
LKGiM1004BH90	11-194	BH		S	
LKGiM1004BH91	11-195	BH		S	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
LKGiM1004BH92	11-196	BH		S	
LKGiM1004BH93	11-197	BH		S	
LKGiM1004BH94	11-198	BH		S	
LKGiM1004BH95	11-199	BH		S	
LKGiM1004BH96	11-200	BH		S	
LKGiM1004BH97	11-201	BH		S	
LKGiM1004BH98	11-202	BH		S	
LKGiM1004BH99	11-203	BH		S	
LKGiM1004BHA0	11-214	BH		S	
LKGiM1004BHA1	11-205	BH		S	
LKGiM1004BHA2	11-206	BH		S	
LKGiM1004BHA3	11-207	BH		S	
LKGiM1004BHA4	11-208	BH		S	
LKGiM1004BHA5	11-209	BH		S	
LKGiM1004BHA6	11-210	BH		S	
LKGiM1004BHA7	11-211	BH		S	
LKGiM1004BHA8	11-212	BH		S	
LKGiM1004BHA9	11-213	BH		S	
LKGiM1004BHB0	11-224	BH		S	
LKGiM1004BHB1	11-215	BH		S	
LKGiM1004BHB2	11-216	BH		S	
LKGiM1004BHB3	11-217	BH		S	
LKGiM1004BHB4	11-218	BH		S	
LKGiM1004BHB5	11-219	BH		S	
LKGiM1004BHB6	11-220	BH		S	
LKGiM1004BHB7	11-221	BH		S	
LKGiM1004BHB8	11-222	BH		S	
LKGiM1004BHB9	11-223	BH		S	
LKGiM1004BHC1	11-225	BH		S	
LKGiM1004BHC2	11-226	BH		S	
LKGiM1004BHC3	11-227	BH		S	
LKGiM1004BHC4	11-228	BH		S	
LKGiM1004BHC5	11-229	BH		S	
LKGiM1004BHC6	11-230	BH		S	
LKGiW7375BHZA	2- 40	BH		B	
LPLTM2356BHZZ	11- 13	AL		C	
LPLTM2357BHZZ	2- 80	AK		C	
LPLTM6723BHZZ	2- 5	AT		C	
LX-BZ6778BHZZ	2- 10	AA		C	
LX-BZ6782BHZZ	2- 1	AA		C	
LX-BZ6787BHZZ	1- 5	AB		C	
LX-BZ6794BHZZ	2- 67	AE		C	
〃	11- 55	AE		C	
【M】					
MHNG-2324BHZZ	1- 9	AX		C	
MHNG-2325BHZZ	1- 11	AX		C	
MLEVF2324BHZZ	1- 4	AG		C	
MSPRE6756BHZZ	2- 15	AQ		C	
MSPRP2372BHZZ	1- 3	AE		C	
【N】					
NFANP6003RCZZ	2- 16	BF		B	
NFANP6004RCZZ	2- 24	BA		B	
【P】					
PCUSG7080RCZZ	2- 69	AH		C	
〃	11- 54	AH		C	
PCUSS2404BHZZ	2- 61	AG	N	C	
PFiLW6979BHZA	1- 49	AX		D	
PGUMM2389BHZZ	1- 8	AE		C	
PGUMM6730BHZZ	1- 33	AS		C	
PGUMM6731BHZZ	1- 28	AR		C	
PGUMM6732BHZZ	1- 30	AS		C	
PGUMM6733BHZZ	1- 29	AR		C	
PGUMM6734BHZZ	1- 32	AL		C	
PRDAF2350BHZZ	2- 18	AR		C	
PRNGT6641BHZZ	3- 15	AE		C	
PSHEG2859BHZZ	1- 38	AV		C	
PSHEG6863RCZZ	2- 19	AR		C	
PSHEP2471BHZZ	1- 45	AH		C	
PSHEP2472BHZZ	1- 44	AH		C	
PSHEP2874BHZZ	1- 56	AH		C	
PSHEP2891BHZZ	3- 16	AF	N	D	
PSHEP6859BHZZ	2- 17	AN		C	
PSPAG2379BHZZ	2- 75	AH		C	
PSPAZ2380BHZZ	2- 31	AD		C	
【Q】					
QACCV6422BHZZ	2- 52	AY		B	
QCNCM2656RC0C	7- 1	AE		C	
QCNCM2788BH0i	4-151	BL		C	
QCNCM2806RC8J	4- 75	AR		C	
QCNCM6467RC4D	4-153	AN		C	
QCNCM7037RCAJ	8- 2	AT		C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
QCNCM7057BH08	4-149	AG		C	
QCNCM7057BHZZ	4-152	AB		C	
QCNCM7126BH2B	8- 1	AN		C	
QCNCM7128BH1E	4-128	AH		C	
QCNCM7142BH1B	4-125	AD		C	
QCNCM7176BH0G	4-123	AD		C	
QCNCM7176BH0H	4-148	AD		C	
QCNCM7176BH1J	4-154	AD		C	
QCNCM7207BH4J	5- 28	AQ		C	
〃	6- 1	AQ		C	
QCNCM7221BH1J	4-126	AL		C	
QCNCM7222BH0C	4-129	AC		C	
QCNCM7226BH0E	6- 2	AD		C	
〃	7- 19	AD		C	
QCNCM7230BH1E	6- 3	AL		C	
QCNCW1230AC3A	10- 1	AK		C	
QCNCW1275AC0F	9- 1	AF		C	
QCNCW2612RCDD	4- 76	AZ		C	
QCNCW2805RC0H	4-150	AU		C	
QCNCW2807RC8J	5- 7	AS		C	
QCNCW2811BH1B	4-147	AK		C	
QCNCW2811BH1F	4-124	AM		C	
〃	9- 2	AM		C	
QCNCW2812BH3J	6- 8	AP		C	
〃	10- 2	AP		C	
QCNCW7040RCAJ	4-130	AT		C	
QCNCW7081BHZZ	4-132	AB		C	
QCNCW7283BH2F	4-155	AS		C	
QCNW-2972BHZA	1- 12	AR		C	
QCNW-2973BHZZ	1- 19	AS		C	
QCNW-2976BHZZ	1- 16	AK		C	
QCNW-2994BHZZ	6- 5	AE		C	
QCNW-2996BHZZ	1- 22	AD		C	
QCNW-3012BHZZ	2- 32	AL		C	
QCNW-3034BHZZ	4-146	AK		C	
QCNW-3056BHZZ	2- 63	AN	N	C	
QCNW-3061RCZZ	2- 52	AS	N	B	
QCNW-7708BHZZ	2- 44	AM		C	
QCNW-7858BHZZ	11- 1	BL		S	
QCNW-7863BHZZ	2- 33	AT		C	
QCNW-7864BHZZ	2- 6	AG		C	
QCNW-7911RCZZ	3- 9	BB		C	
QFS-G4302QCZZ	4-143	AG		A	
QPLGA0006QCZZ	2- 52	AQ		C	
QSŌCZ2036HCZZ	4- 77	AS		C	
QSW-S0744AFZZ	4-141	AG		B	
〃	8- 4	AG		B	
QSW-Z6909BHZZ	9- 3	AF		B	
QSW-Z7011XCZZ	9- 4	AL		B	
QTANP0004BHZA	2- 60	AE		C	
【R】					
RALMB6640RCZZ	4-133	AF		B	
RC-CZ1063RC1A	4- 13	AE		C	
〃	4- 84	AE		C	
〃	5- 3	AE		C	
RC-CZ2201RC0F	7- 2	AE		C	
RC-EZ106ARC1A	4-134	AD		C	
〃	6- 6	AD		C	
RC-EZ1072RC1A	4-136	AN		C	
RC-EZ1572RC0J	4-137	AN		C	
〃	6- 7	AN		C	
RC-EZ2271RC1A	4-135	AM		C	
RC-EZ476ARC1A	4-144	AF		C	
RC-FZ8231RC2A	7- 10	AG		C	
RC-KZ1054CCZZ	6- 4	AB		C	
RCiLC2414RCZZ	4- 78	AH		C	
RCiLC6662RCZZ	4-142	AK		C	
RCiLC6665RCZZ	4- 49	AH		C	
RCiLC6666RCZZ	4- 50	AH		C	
RCiLC6667BHZZ	7- 3	AN		C	
RCiLF0050FCZZ	4-139	AG		C	
RCiLZ1051LCZZ	6- 29	AD		C	
RCiLZ5017SCZZ	4- 24	AB		C	
〃	4- 96	AB		C	
〃	5- 5	AB		C	
〃	6- 9	AB		C	
RCŌRF1008ACZZ	4- 97	AB		C	
〃	5- 17	AB		C	
RCŌRF2031SCZZ	1- 50	AN		C	
〃	2- 13	AN		C	
RCŌRF2327RCZZ	5- 8	AE		C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
RCŌRF2336RCZZ	3- 8	AC		C	
RCŌRF6691BHZZ	4-138	AD		C	
RCŌRF6695BHZZ	2- 51	AK		C	
RCŌRF6706BHZZ	4-140	AD		C	
RCŌRF6712BHZZ	1- 54	AG		C	
〃	2- 27	AG		C	
RCRMZ7002RCZZ	6- 10	AE		B	
RCRMZ7003RCZZ	4- 72	AF		B	
RCRMZ7004RCZZ	4- 71	AE		B	
RCRSZ2402RCZZ	5- 14	AL	N	B	
RCRSZ6670RCZZ	4- 74	AK		B	
RCRSZ6671RCZZ	4- 73	AH		B	
RDENC1014RCZZ	2- 25	BX	N	E	
RMPTQ2103QCJJ	4- 3	AA		B	
RMPTQ2472QCJJ	4- 4	AA		B	
RMPTQ4102QCJJ	4- 5	AB		B	
RMPTQ4103QCJJ	4- 1	AB		B	
RMPTQ4220QCJJ	4- 9	AB		B	
RMPTQ4223QCJJ	4- 7	AB		B	
RMPTQ4330QCJJ	4- 8	AC		B	
〃	5- 1	AC		B	
RMPTQ4472QCJJ	4- 2	AC		B	
RMPTQ4473QCJJ	4- 6	AB		B	
RTRNH9521BHZZ	7- 4	BB		B	
RVR-B5310QCZZ	4-156	AG		B	
【S】					
SPAKA8454BHZA	3- 2	AN		D	
SPAKA8455BHZA	3- 4	AN		D	
SPAKC3049BHSA	3- 1	AX	N	D	
SSAKA5004CCZZ	3- 7	AA		D	
SSAKH0003DHZZ	3- 3	AE		D	
SSAKH3015CCZZ	3- 5	AA		D	
SSAKH4231CCZZ	3- 10	AA		D	
【T】					
TCADH6788BHZA	3- 11	AC		D	
TCAUS6677BHZZ	2- 50	AD		D	
TiNSM2391BHZZ	3- 6	BK	N	D	
TLABG6967BHZZ	2- 48	AC		D	
TLABG7097BHZZ	2- 49	AF		D	
TLABH2460BHZZ	2- 55	AE		D	
TLABH2476BHZZ	2- 37	AE		D	
TLABH6996BHZZ	2- 64	AD		D	
【U】					
UBATN2338RCZZ	2- 45	BE		B	
UBNDA6630BHZZ	3- 12	AK		C	
UKŌG-6705RCZZ	11-104	BC		S	
UKŌG-6717RCZZ	11-102	BR		S	
UKŌG-6718RCZZ	11-103	BE		S	
UKŌG-6729BHZZ	11-106	AZ		S	
【V】					
VCCCTV1HH100J	4- 20	AA		C	
〃	4- 86	AA		C	
VCCCTV1HH101J	4- 79	AA		C	
〃	4- 90	AA		C	
〃	8- 8	AA		C	
VCCCTV1HH150J	4- 17	AA		C	
VCCCTV1HH180J	4- 16	AA		C	
〃	6- 28	AA		C	
VCCCTV1HH220J	4- 21	AA		C	
VCCCTV1HH221J	4- 87	AA		C	
VCCCTV1HH240J	5- 26	AA		C	
VCCCTV1HH270J	4- 18	AC		C	
〃	5- 27	AC		C	
VCCCTV1HH331J	4- 89	AA		C	
〃	6- 11	AA		C	
VCCCTV1HH390J	4- 83	AA		C	
VCCCTV1HH470J	4- 88	AA		C	
〃	5- 20	AA		C	
VCCCTV1HH471J	4-120	AA		C	
VCCCTV1HH681J	6- 12	AA		C	
VCEAGA1HW226M	8- 3	AB		C	
VCEAGU0JW227M	4-145	AB		C	
VCEAPS1CC106M	4- 14	AC		C	
VCEAPS1CC225M	7- 6	AF		C	
VCEAPS1CC226M	7- 7	AC		C	
VCEAPS1CC336M	6- 13	AF		C	
VCEAPS1EC476M	4- 11	AF		C	
VCEAPS1VC226M	4- 12	AC		C	
VCKYTV1CB334K	4- 92	AC		C	
VCKYTV1CF105Z	4- 91	AB		C	
〃	5- 4	AB		C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
VCKYTV1CF105Z	7- 11	AB		C	
VCKYTV1HB102K	4- 19	AA		C	
〃	4- 85	AA		C	
〃	5- 19	AA		C	
〃	6- 27	AA		C	
〃	7- 12	AA		C	
VCKYTV1HB103K	4- 93	AB		C	
VCKYTV1HB182K	6- 14	AA		C	
VCKYTV1HB472K	6- 15	AA		C	
VCKYTV1HF104Z	4- 10	AA		C	
〃	4- 82	AA		C	
〃	5- 2	AA		C	
〃	5- 18	AA		C	
〃	6- 16	AA		C	
VCTZZA0JD157M	4- 15	AN		C	
VHD1SS322//-1	4- 95	AC		B	
VHD1SS353//-1	4- 94	AB		B	
〃	6- 17	AB		B	
VHDSB140///-1	8- 5	AF		B	
VHDSFPB54//-1	4- 23	AC		B	
〃	7- 13	AC		B	
VHDSFPB72//-1	4- 22	AE		B	
〃	4- 99	AE		B	
VHHMiNSMDC020	4- 51	AF		B	
VHi28F004SUT8	4- 42	BA		B	
VHi28F016SU10	4- 39	BU		B	
VHi416V254TL6	5- 9	AX		B	
VHi4AC16///-1	4-131	AK		B	
VHi51V8512T12	4- 34	BG		B	
VHi51W16165A6	4- 45	BE		B	
VHi74HC138DR/	4- 80	AK		B	
VHi74HCT00ANS	5- 12	AH		B	
VHi74HCT08ANS	5- 11	AE		B	
VHi74HCT244AF	5- 10	AK		B	
VHi74VHC04/-1	4- 38	AE		B	
VHi82C700P/-1	4- 44	BT		B	
VHiA80502-133	4-127	CS		B	
VHiBA10393F-1	4- 81	AC		B	
VHiBQ3285ESS1	4- 41	AW		B	
VHiLH535DVC-1	4- 40	BA		B	
VHiLT1184CS-1	7- 5	BE		B	
VHiLZ9AM22/-1	4- 28	BH		B	
VHiM38802M270	4- 33	BA		B	
VHiM5113A2QFP	4- 31	BB		B	
VHiM89635N010	6- 18	BA		B	
VHiMAX1651/-1	4- 47	AS		B	
VHiMAX797CSE/	4- 43	AZ		B	
VHiMC14069UBD	4- 26	AK		B	
VHiMC145406F1	4- 25	AL		B	
VHiMK1492-04R	4- 46	AY		B	
VHiMN89305/-1	5- 13	BG		B	
VHiRH5RE33A-1	4- 48	AF		B	
VHiRN5VL45CA1	4- 29	AF		B	
VHiS29390AFJA	6- 19	AL		B	
VHiSN74HC00DR	4- 36	AG		B	
VHiSN74HC04DR	4- 32	AG		B	
VHiSN74HC08DR	4- 37	AL		B	
VHiSN74HC32DR	4- 35	AG		B	
VHiSN74LS125R	4- 27	AL		B	
VHiSN75189DR/	4- 30	AK		B	
VHViCPS0.5/-1	7- 14	AF		B	
VHViCPS1.0/-1	4- 98	AF		B	
〃	5- 6	AF		B	
VRS-TQ2BB000J	6- 20	AA		C	
VRS-TS2AD000J	4- 65	AA		C	
〃	4-107	AA		C	
VRS-TS2AD102J	4-108	AA		C	
〃	5- 23	AA		C	
〃	6- 21	AA		C	
VRS-TS2AD103J	4- 58	AA		C	
〃	4-104	AA		C	
〃	5- 21	AA		C	
〃	6- 22	AA		C	
〃	8- 7	AA		C	
VRS-TS2AD104J	4-116	AA		C	
〃	7- 15	AA		C	
VRS-TS2AD105J	4- 64	AA		C	
〃	4-119	AA		C	
VRS-TS2AD106J	4- 59	AA		C	
VRS-TS2AD122J	4-112	AA		C	
VRS-TS2AD133F	7- 8	AA		C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
VRS-TS2AD144F	4- 69	AC		C	
VRS-TS2AD152J	4-113	AA		C	
VRS-TS2AD154F	4- 68	AA		C	
VRS-TS2AD183J	5- 25	AA		C	
VRS-TS2AD203J	6- 23	AA		C	
VRS-TS2AD220J	4- 60	AA		C	
〃	4-105	AA		C	
VRS-TS2AD222J	4-121	AA		C	
〃	7- 16	AA		C	
VRS-TS2AD223J	4-115	AA		C	
VRS-TS2AD224J	7- 17	AA		C	
VRS-TS2AD270J	4-114	AA		C	
VRS-TS2AD272J	4-109	AA		C	
〃	8- 6	AA		C	
VRS-TS2AD330J	4- 63	AA		C	
〃	4-106	AA		C	
〃	5- 22	AA		C	
VRS-TS2AD332J	4-111	AA		C	
VRS-TS2AD333J	5- 24	AA		C	
VRS-TS2AD334J	5- 15	AA		C	
VRS-TS2AD470J	4- 61	AA		C	
VRS-TS2AD471J	4- 57	AA		C	
〃	4-103	AA		C	
VRS-TS2AD472J	4-122	AA		C	
〃	7- 9	AA		C	
VRS-TS2AD473J	4-110	AA		C	
VRS-TS2AD474J	4- 62	AA		C	
VRS-TS2AD682J	4- 56	AA		C	
VRS-TS2AD751J	4-118	AA		C	
VRS-TS2AD822J	4-117	AA		C	
〃	6- 24	AA		C	
VRS-TS2HD130J	4- 70	AD		C	
VRSTE2HFR025F	4- 66	AE		C	
VRSTE2HFR033F	4- 67	AE		C	
VS2SD2391//-1	7- 18	AD		B	
VS2SJ187-//-1	4-102	AF		B	
〃	5- 16	AF		B	
VSDTA124EK/-1	6- 25	AD		B	
VSDTA144EK/-1	4- 52	AC		B	
VSDTC114YK/-1	4- 53	AC		B	
〃	4-100	AC		B	
VSDTC124GK/-1	4-101	AC		B	
VSDTC124TK/-1	6- 26	AD		B	
VSSi9410DY/-1	4- 54	AK		B	
VSSi9430DY/-1	4- 55	AL		B	
VVLLM10V33/-1	1- 26	CS		B	
【X】					
XBBSD30P04000	2- 7	AA		C	
〃	3- 17	AA		C	
XBBSD30P06000	2- 74	AA		C	
XBBSD30P08000	1- 43	AA		C	
XBPBZ40P06K00	2- 28	AA		C	
XBPSD30P08KS0	2- 77	AA		C	
XEBSD30P06000	1- 52	AA		C	
XEBSD30P08000	1- 15	AA		C	
〃	2- 2	AA		C	
XEBSD30P10000	2- 59	AA		C	
XEBSD30P20000	2- 23	AA		C	
XEPSD30P08000	1- 18	AA		C	
XHBSD30P05000	1- 14	AA		C	
XHBSD30P06000	2- 20	AA		C	
XJBSF30P10000	2- 47	AA	N	C	
XJSSD26P08000	2- 58	AA		C	
XJSSD30P08000	1- 39	AA		C	
XJSSD30P10000	1- 6	AA		C	
XUBSD40P08000	1- 10	AA		C	
XUBSD40P12000	1- 51	AA		C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	

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